

Alumina & Leaded Molded Technology 3

3.1 Introduction

The packaging technologies used to manufacture or assemble three basic types of component packages are summarized in this chapter.

The package families, described in Chapter 1, provide the functional specialization and diversity required by device and product applications. Material and construction attributes of individual family members are provided by the following package technologies: (1) fired ceramic, (2) pressed ceramic, and (3) molded plastic. Intel's packaging technology using organic substrates will be discussed in chapters 13, 14, and 15. Cartridge packaging assembly will be discussed in Chapter 16.

Each of the three package families described in this chapter have some similar process steps but, the packaging materials and the form factors are uniquely different.

The assembly core technology process steps (die attach, wire bond, lid seal, finish) are most commonly used in the industry today. However, several form factor modifications, driven on one hand by the advent of "Surface Mount Technology" (Quad Flat Pack packages and Ball Grid Array) and on the other hand by area array package socketing requirements (Pin Grid Array) are now the more commonly used form factors for microprocessors.

This chapter will review in detail those core packaging technologies that are common to most of the standard IC package family types, i.e. DIPs, QFPs & Ceramic PGAs.

3.2 Die Preparation

Intel's die preparation consists of wafer mount and wafer saw process. Intel protects the active surface of wafers from handling-induced defects by using a contactless wafer mounting process. The wafer is mounted to a mylar tape to ensure the die is in place during and after sawing process. The mounted wafer is sawn into singulated die followed by high pressure deionized (DI) water wash. The wafer wash process is properly characterized to ensure no silicon dust and static charge build-up which will induce passivation damage. Intel uses 100% wafer saw through process to prevent die chipping.

3.3 Die Attach

For these packages Intel uses two categories of die attach adhesive materials: (1) adhesives, both organic and inorganic; and (2) hard solders (gold-silicon eutectic). The choice of die attach material depends on the specific applications and its compatibility with the particular packaging technologies to ensure the highest levels of reliability performance. Table 3-1 and Table 3-2 summarize the die attach materials used by package technology.

Table 3-1. Die Attach Materials by Package Technology

Package Technology	Die Attach Material	Type
Pressed Alumina Ceramic (CERDIP)	Silver-Filled Glass	Inorganic Adhesive
Laminated Alumina Ceramic (PGA, CQFP, Side-Braze)	Gold-Silicon Eutectic Silver-Filled Cyanate Ester	Hard Solder Organic Adhesive
Molded Plastic	Silver-Filled Epoxy	Organic Adhesive

Table 3-2. Die Attach Material Summary

	Au-Si	Silver-Filled Glass	Silver-Filled Epoxy/ Cyanate Ester
Wafer Backside Metallization for Die Attach	Required	Not Required	Not Required
Wafer Backside Metallization for Ohmic Contact	Not Required	Required	Required
Thermal Dissipation	Good	Good	Fair
Electrical Conductivity	Good	Good	Fair
Lead Frame Compatibility	N/A	N/A	Good
Substrate Metallization Compatibility (a) Gold (b) Silver (c) Al ₂ O ₃	Good Good N/A	Poor Good Good	Good Good N/A

Figure 3-1 through Figure 3-4 are schematic cross-sections through each of the different die attach systems currently in use at Intel, for example, gold/silicon eutectic, silver-filled glass, and silver filled organic adhesives, epoxy, and cyanate ester. The components of each system are identified.

Figure 3-1. Gold-Silicon Eutectic

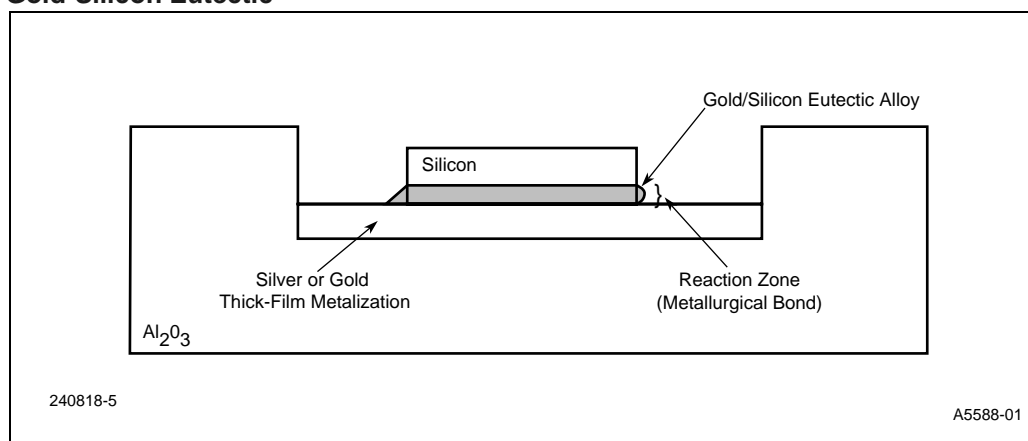


Figure 3-2. Silver-Filled Glass

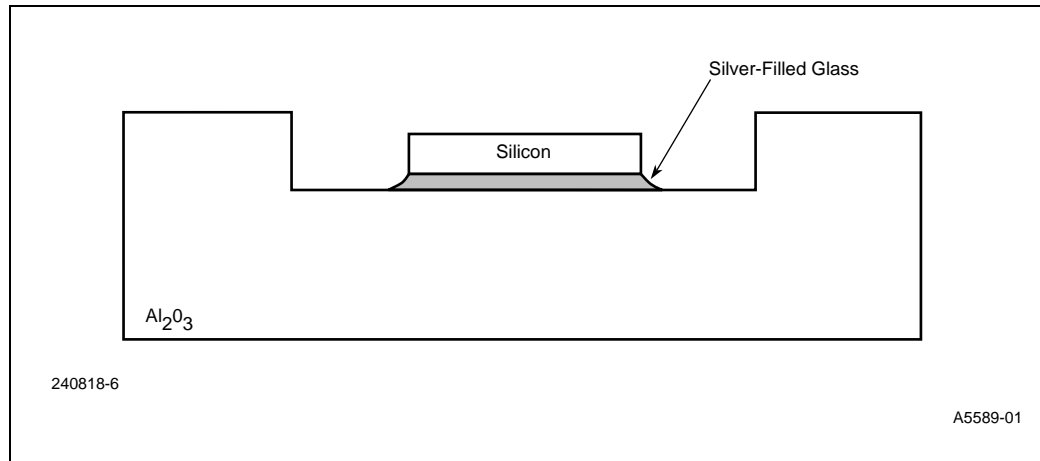


Figure 3-3. Silver-Filled Cyanate Ester

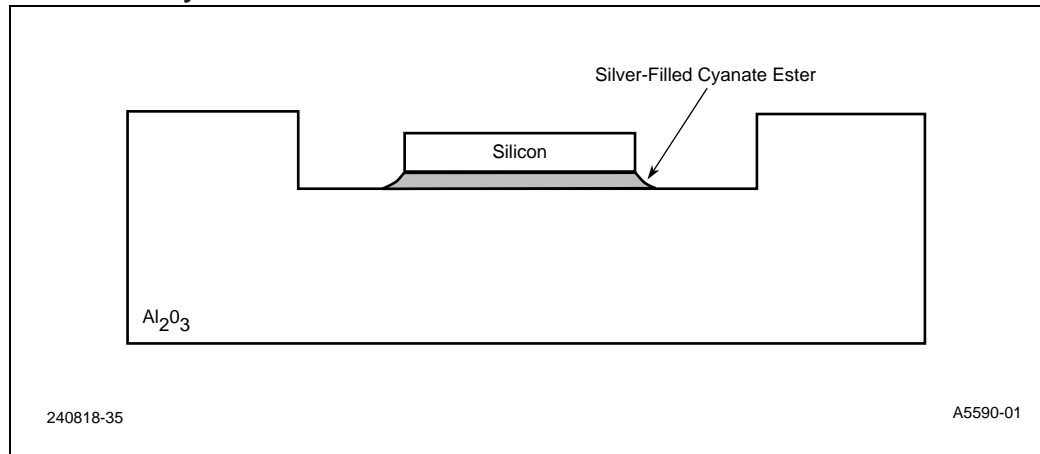
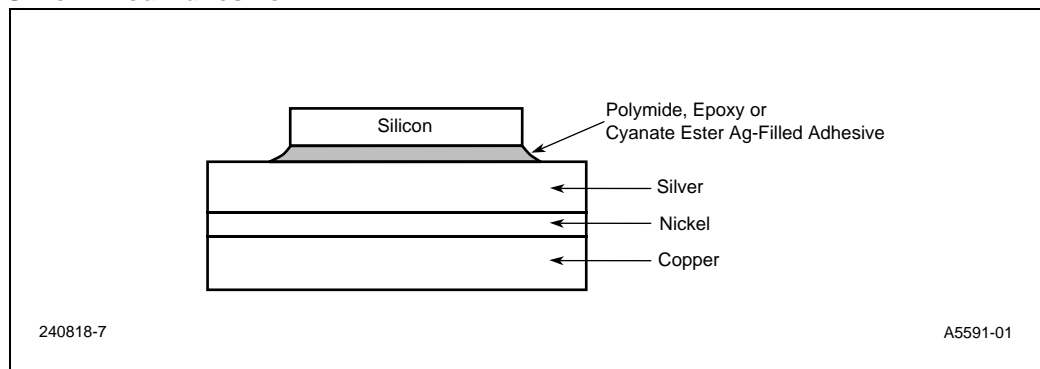


Figure 3-4. Silver-Filled Adhesive



3.3.1 Purpose of Each Component

Wafer metallization provides an ohmic contact to the silicon die for the purpose of substrate biasing for those die attach media that do not readily form an ohmic junction. It provides a readily wettable surface for gold/silicon hard soldering and prevents premature oxidation (or aging) of the wafer backside during storage by acting as a diffusion barrier, thus ensuring that die attach integrity remains uncompromised.

Like the wafer backside, **substrate metallization** provides a readily wetted surface for hard soldering. Metallizations used in hermetic package technologies, both gold and silver, are readily wetted by the liquid solder at die attach temperatures and actually react with the solder to provide a high-integrity metallurgical bond to the substrate. Both substrate metallizations resist oxidation, which can impede wetting, and are electrically conductive for those devices that require electrical contact.

Plastic packages use a plated silver metallization to adhere to organic adhesives, which are electrically conductive. Silver-filled glass does not require a metallization, though it will adhere readily to silver.

Die attach media serve several purposes other than the obvious one of attaching the silicon to the substrate. They also provide a means of making an electrical connection to the die backside for those devices requiring it, as well as a path for the conduction of heat from the die to the ambient. For these reasons, the die attach media used at Intel exhibit good thermal and electrical conductivity.

The incoming quality of die attach materials is monitored through a series of specifications unique to each of the die attach media. Tests are performed to measure those specific characteristics necessary to ensure that materials meet the requirements of die attach applications.

3.3.2 Die Attach Process Consideration

From a process design standpoint, it is necessary to understand the limitations of each die attach process. Every die attach technology used at Intel has its own limitations and merits. The materials and process must be carefully characterized to ensure good package compatibility, reliability and manufacturability.

3.3.2.1 Au-Si Eutectic

There are three key considerations to the Au-Si Eutectic process. Foremost is the effect of processing temperature on die reliability and performance. It is necessary to design the silicon fabrication processes so that the device can withstand the Au-Si process temperatures during die attach. Next is the need to have good die backside metallization for high reliability performance. All wafers used in this process use a gold wafer backside metallization. The third consideration is the need for an excellent process control.

3.3.2.2 Silver-filled Glass (SFG)

SFG, like Au-Si eutectic, is limited to those devices which can withstand SFG processing temperature and time. The silicon fabrication processes should be designed to withstand the die attach process. Because of the organic content (solvent and resin binder) of the SFG paste, its removal is necessary for good adhesion. The larger the die, the longer is the drying/processing time for organic content removal.

There are also limits to the bond line thickness, both thin and thick, that constrain the process. In addition, it is imperative to maintain a nearly void-free die attachment. SFG is limited to (1) non-gold wafer backsides and substrates due to poor adherence to gold, and (2) inert or oxidizing processing ambients.

Like Au-Si eutectic, SFG requires close process control. Once processed, the SFG material is stable to extremely high temperatures.

3.3.2.3 Silver-filled Epoxy/Cyanate Ester

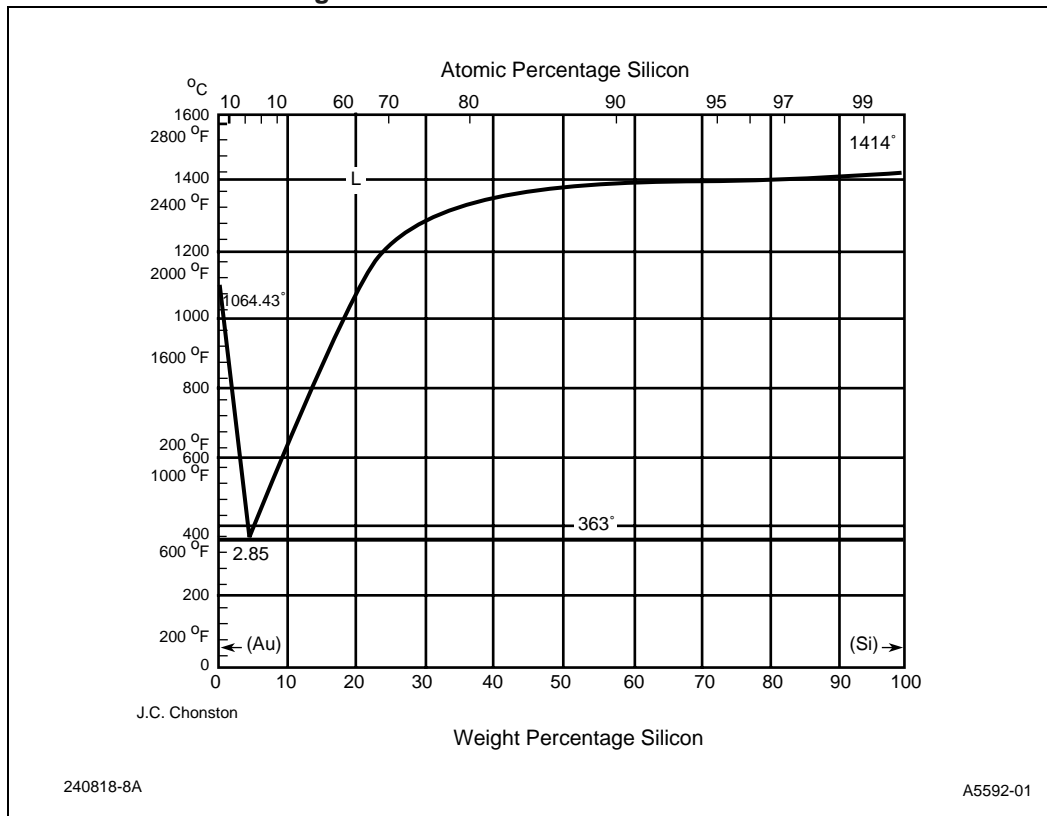
There are two significant considerations for epoxy and cyanate ester adhesives: the first is the upper temperature that the material can tolerate before decomposition of the polymer occurs, which is approximately 200°C for epoxy and 380°C for cyanate ester. The second is the optimum bond line thickness control, again a die stress-related concern. As with the other paste technologies, it is important to maintain a nearly void-free die attachment through control of the dispensed paste volume and pattern, coupled with a good curing temperature profile.

3.3.3 Processes

3.3.3.1 Au-Si

Figure 3-5 is a representation of the gold-silicon phase diagram. In this process, a pure gold preform is placed into a preheated ceramic package under a heated inert gas. The die is placed onto the preform and allowed to reach the preset die attach temperature.

Figure 3-5. Gold-Silicon Phase Diagram



As the temperature is raised, silicon from the die begins to diffuse through the diffusion barrier on the die backside, and at 363 °C it forms eutectic composition liquid. Once liquid formation occurs, the reactions proceed rapidly by liquid phase diffusion. As the temperature increases beyond the eutectic temperature, more silicon is dissolved from the die backside until the equilibrium volume of silicon is reached. The liquid also begins to dissolve the gold or silver substrate. The amount of gold or silver that dissolves depends on the temperature and the time of die attach.

Once the liquid is evenly distributed across the silicon backside to ensure intimate contact with all areas, the package and die are cooled. During cooling, silicon begins to precipitate from the saturated gold-silicon liquid. These precipitates grow epitaxially from the silicon die backside. Analysis using a transmission electron microscope has confirmed that the epitaxial region is continuous with the bulk silicon crystal structure. When the package again reaches the eutectic temperature, the solder solidifies with a characteristic eutectic-type microstructure. There is no solid solubility of silicon in gold or vice versa, as evidenced by the phase diagram for the system. The joint obtained upon cooling is metallurgically continuous from the substrate to the die.

3.3.3.2 Silver-filled Glass

Silver-filled glass is a suspension of silver and low-softening temperature glass particles in an organic vehicle. In this process, the paste is automatically applied to the ceramic via a paste dispense system. After the paste is applied, the die is positioned within the dispensed pattern. Because of the high organic content of the paste, the SFG is carefully dried in a continuous furnace to remove the solvent (the presence of solvent will lead to poor adhesion to die). This leaves behind a resin that binds the silver and glass particles until subsequent processing can soften the glass. After drying, the material is carefully heated to remove the binder; the heating rate is determined by die size.

At higher temperatures, the glass begins to soften, and the silver particles begin to sinter together into a cohesive mass. Considerable shrinkage accompanies the reactions at higher temperatures, and care must be taken to ensure that the minimum bond line thickness requirements are maintained after shrinkage. At the highest temperature, the glass wets the silver particles, silicon surface, and ceramic substrate, creating a strong chemical bond between the silicon and the ceramic. Once the material has reached the maximum density, the package is cooled and readied for subsequent assembly operations.

3.3.3.3 Silver-filled Epoxy/Cyanate Ester

Silver-filled epoxy/cyanate ester used by Intel is a solventless system, which eliminates the processing issues associated with drying. Because of the chemical structure of these adhesives, water vapor evolution during process is also not a concern. As with the other paste technologies (polyimide and SFG), the paste is automatically dispensed and the die is positioned with automated equipment, with care taken to ensure a void-free die attach. After placement, the package is heated to the epoxy resin cure temperature to polymerize the epoxy/cyanate ester and create the final chemical bond between the silicon and lead frame or substrate.

3.3.3.4 Backside Requirements and Controls

The wafer backside process can affect the integrity of the joint created during die attach. From gold-silicon eutectic work, it has been determined that a metallized surface is required for highly reliable joining. The quality of the metallization modulates the wetting of the liquid to the silicon and enhances the quality of the braze joint. Surface roughness plays a significant role in eutectic die attach; smooth surfaces wet more readily and more quickly than rougher ones.

To prevent premature oxidation of the metallization, a diffusion barrier is necessary. The barrier is required to adhere to both silicon and gold, yet not interfere with the integrity of the final joint. The barrier kinetics also must allow rapid diffusion of silicon at the die attach temperatures. Because of this, it is necessary to control the thickness of the barrier metal. The gold thickness must also be controlled to prevent oxidation of the barrier metal.

3.3.3.5 Ohmic Contact

Some MOS devices require an ohmic contact to the die backside. To achieve an ohmic contact, a metallization is required for all paste technologies, as the silver will not form a low-resistance ohmic contact at any of the die attach times or temperatures. An ohmic contact can be achieved with gold-silicon eutectic die attach without the use of a metallization, as the gold readily diffuses at the die attach temperature, creating a low-resistance contact. A wafer backside metallization is necessary for the creation of a highly reliable eutectic joint.

3.3.4 Performance and Engineering Characteristics

3.3.4.1 Die Size Limitations

- **Au-Si.** Larger dies can be attached with this technique. Dies as large as 1.8 x 1.8 cm (0.7 x 0.7 in.) have been successfully attached by this technique.
- **Silver-Filled Glass.** Within Intel it has been demonstrated that dies as large as 1.0 x 1.0 cm (0.4 x 0.4 in.) can be successfully attached by this technique.
- **Silver-Filled Epoxy/Cyanate Ester.** Because there are no limitations on solvent or water vapor evolution for this type of paste, there are no known die size limitations. Dies as large as 1.3 x 1.3 cm (0.6 x 0.6 in.) have been successfully attached using this die attach material.

3.3.4.2 Joint Strengths

Table 3-3 summarizes the die attach joint strengths for each die attach material used at Intel today. As shown, measured strengths easily exceed the military specification for die attach strength as determined by tensile testing.

Typical failure modes related to the die attach process are die cracking and cohesive failure at die attach interface. Intel's die attach process is characterized to prevent these failures. A round tip die ejector die attach pick up process is used to avoid die backside damage. Intel's die attach nozzle and dispensing setup is designed for optimum adhesive coverage with minimum die attach void.

Table 3-3. Typical Tensile Bond Strengths of Various Die Attach Media

Die Attach Media	Tensile Strength (kg/cm ²)	Tensile Strength (psi)
Au-Si	500	>7000
Silver-Filled Glass	100	1400
Silver-Filled Epoxy	140	2000
Silver-Filled Cyanate Ester	140	2000

3.3.4.3 Backside Metallization Controls

Control of the wafer backside metallization process is essential for high-integrity gold-silicon eutectic bonds. As mentioned, it is important to control the thickness of both the barrier metal and the gold. It is also necessary to control the deposition conditions to minimize the oxygen content of the barrier metal. Failure to do so can result in a poorly wettable surface that does not allow rapid, uniform silicon diffusion at the Au-Si die attach temperatures.

3.4 Wire Bonding

Wire bonding is an assembly step that connects the input/output of the device to the package terminals. The thermosonic gold wire bonding and ultrasonic aluminum or gold wedge wire bonding are two common bonding techniques used. At this assembly process stage, the majority of the final cost is already in the device. Thus, it is critical that the highest yield of wire bonding is achieved. The utilization of either wedge or ultrasonic bonding basely dependence of wire pad pitch capability. The former capability will be able to support finer pad pitch up to 65um.

To a achieve a high-quality wire bond, bonding parameters, piecepart material property and bond pad metallization integrity must be well understood and controlled.

Intel works closely with wafer fab process development teams and wire and lead frame/ceramic package vendors to obtain required characteristics for wire, leadframe/package and bond pad metallization.

Critical parameters for wires are diameter, tensile strength, elongation, chemical composition and surface contamination.

Key bond pad characteristics include surface hardness, roughness, cleanliness (freedom from glass residues, oxide and silicon dust), and metallization integrity. The consistency of piecepart materials properties is essential for a high yield and reliable bond process.

3.4.1 Bond Quality Monitors

Intel uses a variety of techniques for measuring the quality and reliability of bonds. The most frequently used techniques are:

- Visual inspection
- Bond pull
- Bond shear test
- Bond etching
- Electrical testing
- Baking test
- Thermal cycling stress
- Surface analysis

3.4.1.1 Visual Inspection

Visual inspection is used to monitor bond quality. Problems that could occur are smashed bonds, small bonds, breaking wires, off-pad and cratering.

3.4.1.2 Bond Pull

The bond-pull test is a primary method used for optimizing the bonding window and monitoring the bond quality. The pull test is influenced by package configuration and wire length. Test results include bond strength and mode of failure.

3.4.1.3 Shear Strength

Intel optimizes bond adhesion strength of gold ball bonds by using the shear strength test. The failure mode and bond strength are used to measure the ball bond quality and reliability.

3.4.1.4 Bond Etching

Bond etching measures the condition of layers under the bond pads after bonding. With this technique, the ball (wire) and pad metallization is removed, and the underlayer materials are examined for defects.

3.4.1.5 Electrical Testing

Electrical testing measures the quality of the bond. A non-sticking bond will result in an electrical open, while two adjacent bonds in contact will result in an electrical short.

3.4.1.6 Bake Test

Bake test measures the degree of intermetallic compound formation of gold-aluminum (Au/Al). Over diffusion of aluminum atoms into gold can lead to Kirkendall voiding at the gold and aluminum interface resulting in bond lifting. Bake test will be done normally followed by electrical test and/or bond pull.

3.4.1.7 Thermal Cycling Stress

Thermal cycling measures reliability of wire bond integrity through accelerated and extreme environment condition. Thermal cycling accelerates bond pad fracture, bond lifting, and metal lifting due to bonding process deficiency or package configuration. Thermal stress will be done normally followed by electrical test and/or bond pull.

3.4.1.8 Surface Analysis

Surface analysis techniques such as energy-dispersive X-ray analysis (EDX), wave-length dispersive X-ray analysis (WDX), Auger, and scanning electron microscopy (SEM) are some failure analysis tools Intel uses to identify the (1) presence of contamination, (2) extent of intermetallic compound formation, bond metalization surfaces and (3) bond irregularities.

3.5 Plastic Molding Process

The technology advancement of molding compound, transfer molding, and package design have made it possible for Intel to manufacture highly reliable plastic component packages.

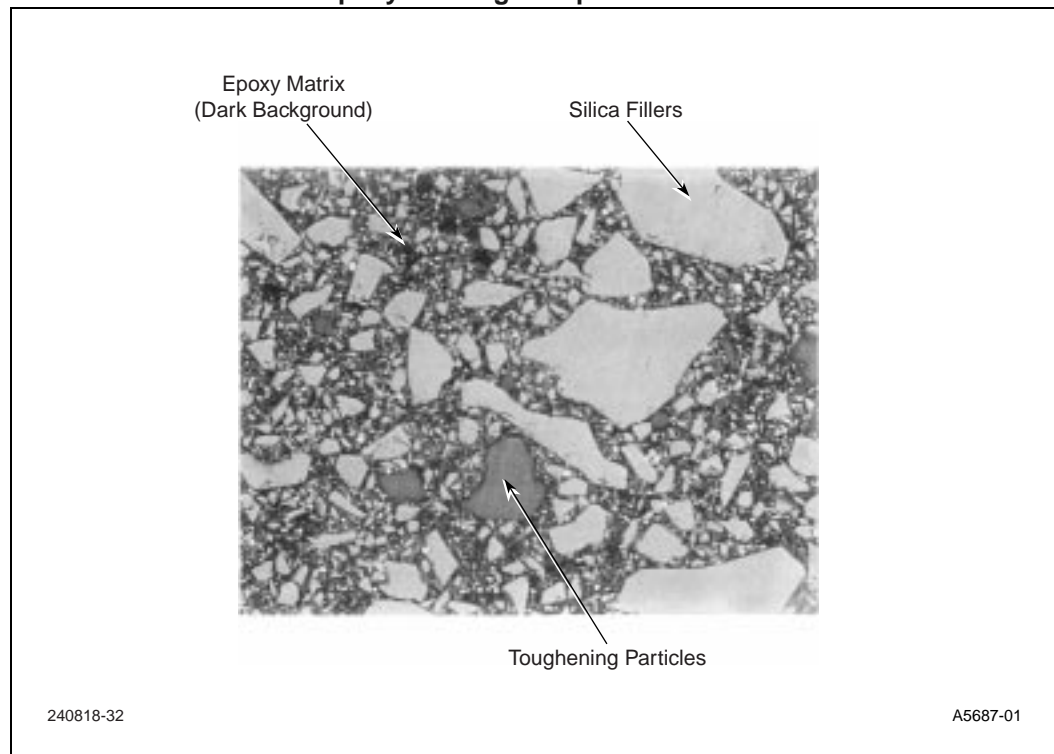
3.5.1 Molding Compound

Molding compound is a composite material, with each component providing a set of properties critical to the overall performance of the system.

The composite matrix material used in Intel packages is an epoxy cresol novolac polymer. This crosslinked material is dimensionally stable, ionically clean, and resistant to assembly process and field-use temperatures. The composite's largest component by weight is silica filler, added to provide control of thermal expansion coefficient, thermal conductivity and enhance the material toughness. The molding compound was also designed for moisture resistance and manufacturability. Intel optimizes the silica filler size and shape to give better flow property, die tool wear resistance and moisture resistance property.

The molding compound consists of elastomeric toughening fillers, flame retardants, coupling agents to improve adhesion between matrix and filler, and release agents to allow removal of the product from the mold. Figure 3-6 is a scanning electron micrograph showing the epoxy molding compound structure.

Figure 3-6. Cross Section View of Epoxy Molding Compound



3.5.2 Molding Process

Intel suppliers provide partially reacted epoxy molding compound in the form of pelletized powder preforms. The epoxy is processed in a transfer molding press which drives the compound through the heated mold. The molding compound viscosity decreases as it contacts a heated mold, allowing it to flow easily around the bonding wires and to fill the package cavity. Viscosity increases as the curing reaction takes place, until the molding compound is hard enough to be removed from the

mold. A schematic plot of molding compound viscosity as a function of time is shown in Figure 3-7, where T_2 is greater than T_1 . Figure 3-8 outlines the primary steps in the transfer molding process.

Figure 3-7. Molding Compound Viscosity—Time Behavior (Schematic)

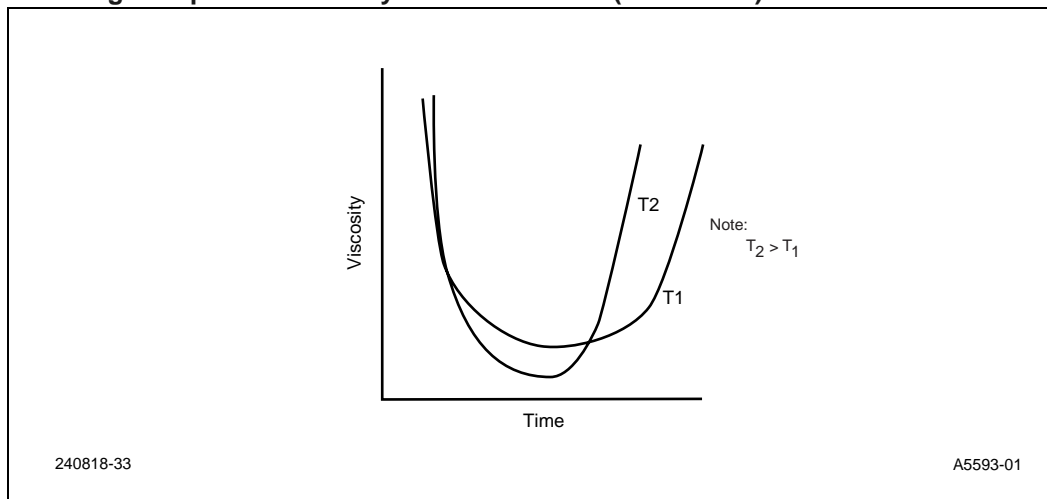
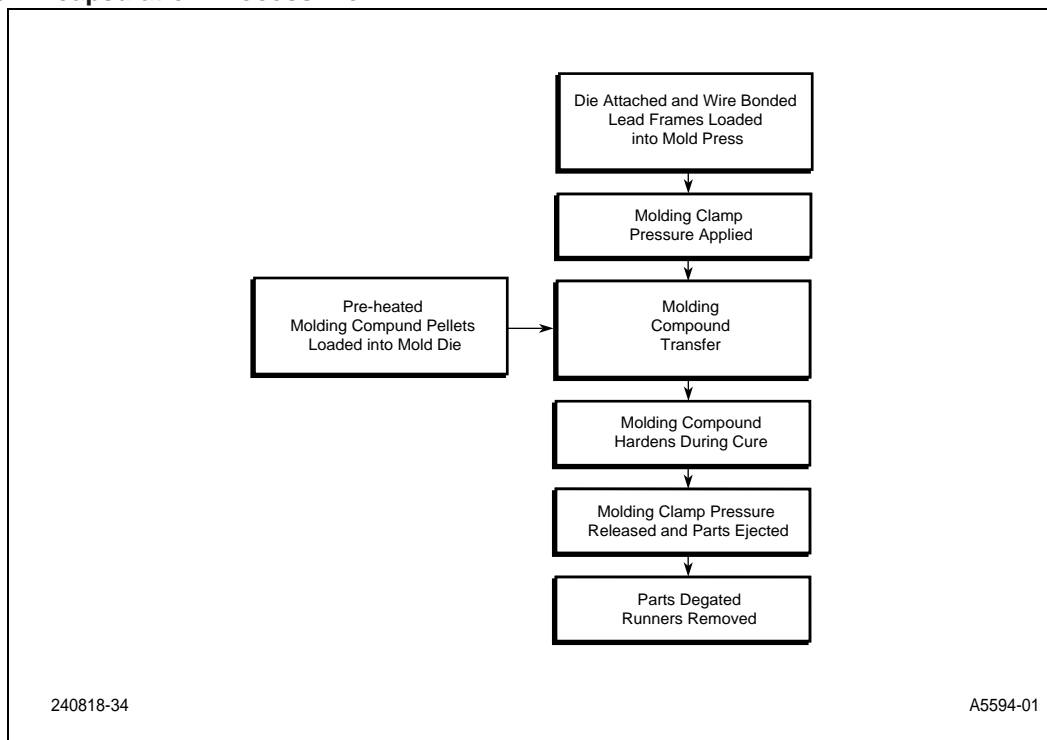


Figure 3-8. Encapsulation Process Flow



Molding process parameters such as cure temperature, compound transfer rate, and cure time are controlled to ensure quality and reliability of a molded package. Of equal importance are the designs of the mold runner and gate systems, the path through which the molding compounds enter the package cavity. Potential defects seen if encapsulation process is not optimized such as

incomplete encap fill, encap void and wire sweep. Intel uses design of experiments (DOE) methodologies that include these variables throughout the development and optimization of the molding process.

3.5.3 Packaging Reliability Considerations

The molded plastic is a composite system composed of:

- A copper alloy lead frame
- Silver-filled polymeric die attach adhesive
- Silicon chip
- Gold bonding wires
- Epoxy molding compound

Each of these components has a unique set of physical properties, and mismatches of these properties, such as the coefficient of thermal expansion, elastical modulus will present a challenge to maintain the mechanical integrity of the bulk materials and the interfaces between them.

Because of different rates of expansion and contraction, stresses concentrate at the interfaces between materials during the temperature cycle as seen in accelerated reliability testing and circuit board mounting. When these stresses exceed the interfacial strength between materials, package delamination or cracking can occur. The presence of absorbed moisture in the molding compound exacerbates this phenomenon during surface mount process.

Precautions are taken to prevent failure of the encapsulant during processing, testing, and application ambient. From the material perspective, the supplier of the molding compound synthesizes the polymer to exhibit minimum moisture absorption. In addition, coupling agents are used to maximize adhesion between the epoxy matrix and silica filler to limit moisture ingress. Optimization of other material properties, such as flexural strength, modulus, and toughness, ensures that the material can perform under severe moisture and temperature-cycling conditions without the occurrence of delamination or cracking, which can lead to the ingress of corrosion-causing contaminants. The molding compound contains elastomeric toughening agents that curtail the growth of cracks should they occur. These “low-stress” materials also provide protection to the fragile chip surface by preventing cracking and shear deformation of the thin-film structures that make up the circuitry.

Careful package and process designs also ensure integrity of the molded package. Package engineers employ design features that enhance component robustness by creating mechanical interlocks between molding compound and lead frame. Assembly process engineers design material flows that maximize adhesion and limit exposure to moisture during manufacturing, shipping, and board mounting.

3.6 Lead Finish

Intel provides three basic lead finishes:

- Gold Plate
- Solder Coat
- Solder Plate

Each type of lead finish offers advantages for specific applications and for internal processing.

3.6.1 Gold Plate

Gold-plated finish is recommended for socket applications only. Package types which use gold plated leads include the ceramic laminate family, including pin grid arrays (PGAs), side-braze dual in-line packages (DIPs), and both leaded and leadless chip carriers.

Previously, gold was considered a universally superior lead finish because of its solderability and electrical and nonoxidizing properties. Over the past several years, however, it has been determined that soldering gold-plated component leads directly into a PC board has disadvantages. Excess gold in the solder joints can result in the formation of a brittle alloy, causing the joints to fail over time in high-vibration or board-flexing environments.

For example, in military applications requiring leadless chip carrier mounting, such considerations become critical. Currently, military requirements demand a solder coated part, replacing gold in direct soldering used for both leadless and leaded components. Gold plating remains the lead finish of choice for socketed units.

3.6.2 Solder Coat

Solder coat components offer the distinct advantages of a low melting point (183°C) and resistance to aging.

The composition of solder coat is the eutectic alloy of 63% tin and 37% lead. Intel normally applies the coating in the following sequence: (1) cleaning the leads, (2) applying a flux, (3) dipping the leads into molten solder, and (4) finishing with a hot water rinse. Great care is taken to minimize any thermal shock to the package and die during solder coat processing and cleaning of the unit after coating. Controlling the temperature profile is important to minimize the thermal stress build-up in the package.

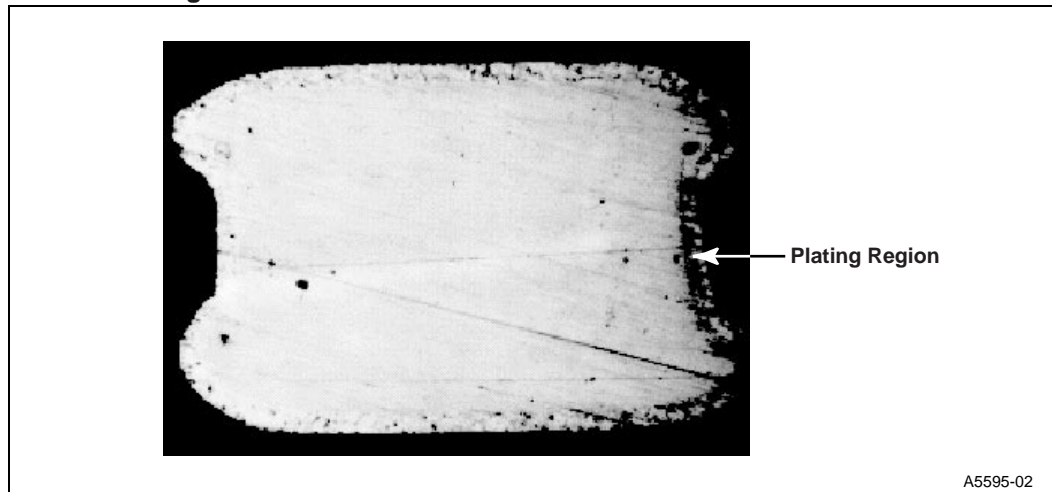
Intel provides solder coat lead finish mostly on plastic and ceramic DIPs for commercial products. The customer can use this lead finish in a variety of PC board assembly processes, including wave soldering, infrared, and vapor phase.

3.6.3 Solder Plate

Intel uses tin-lead alloy plating for plastic quad fine-pitch, quad flatpack, and PLCC packages.

The solder uses co-deposited elements from an alloy composition of 85% tin and 15% lead. As shown in Figure 3-9, the plating on the packages with copper lead frames, with a minimum thickness of 200 microinches, provides full coverage of the copper without exposing any formed intermetallics to the air. At the same time, solder plate produces a very solderable finish with a melting point of approximately 215°C. Like tin-plated leads, those plated with tin-lead alloy can be directly soldered using infrared, vapor phase or socket form.

Figure 3-9. Solder Plating on a Lead Frame



3.6.4 Lead Finish Process Flow

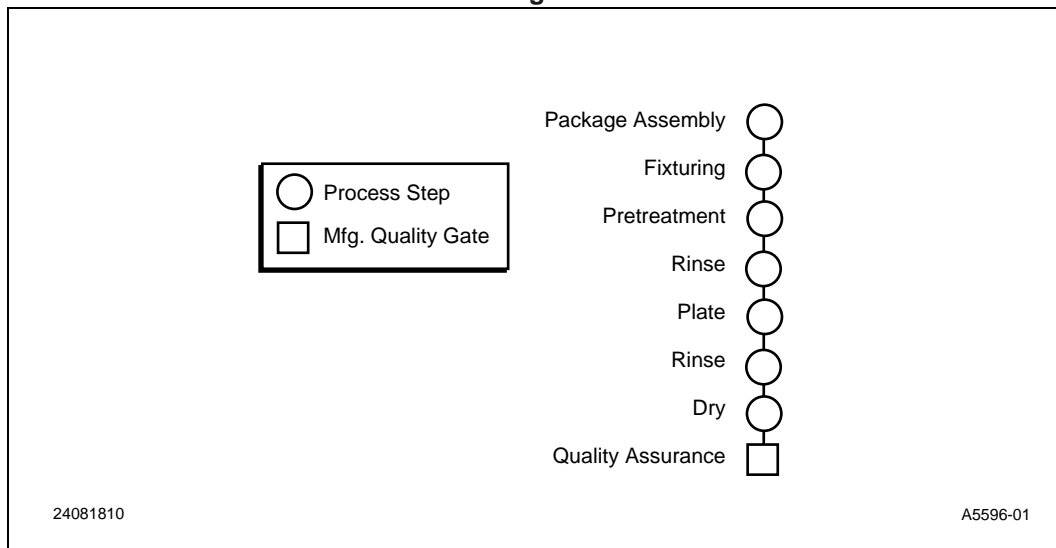
The following sections illustrate the process flow for each type of Intel lead finish.

3.6.4.1 Gold

Packages with gold lead finish are purchased from the package vendor as raw piece parts.

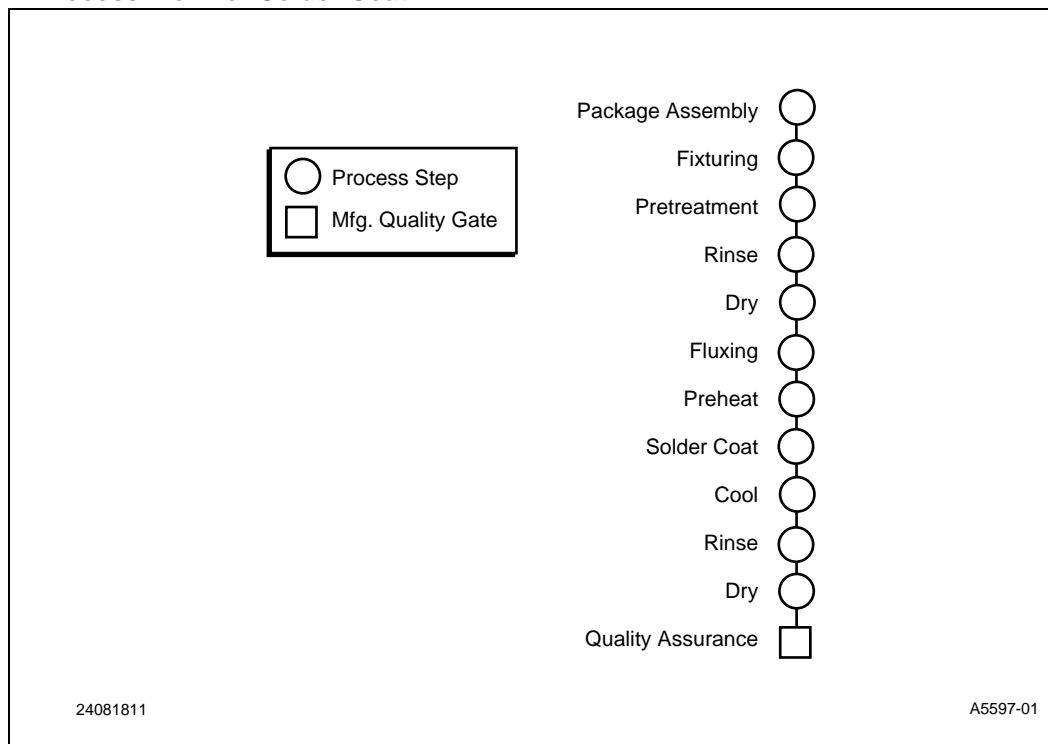
3.6.4.2 Solder Plate

Figure 3-10. Process Flow for Tin and Solder Plating



3.6.4.3 Solder Coat

Figure 3-11. Process Flow for Solder Coat



3.6.5 Process Controls

The plating process is controlled by monitoring a combination of several input and output parameters such as:

- Physical arrangements and condition of the plating anodes and fixtures, as well as distance to the part to be plated.
- Chemical analysis and control of solutions in pre-treatment, plating and rinsing baths.
- Plating parameters such as temperatures, rinse flows, voltage, current density and process times.
- Output quality such as solder thickness, composition, solderability and appearance quality.

The solder coat process is controlled and monitored for:

- Physical height of the solder and condition of fixtures.
- Chemical analysis and control of solutions in pre-treatment, solder bath and rinsing bath.
- Process parameters such as conveyor speed, flux density, preheat temperature, solder temperature and package temperature profile.
- Output quality such as solder thickness, composition, solderability and appearance quality.

3.6.5.1 Lead Forming

Lead forming is a twofold assembly operation that bends and trims plated or solder-dipped leads to meet specified dimensional accuracy. Leads can be formed into three standard configurations: gull-wing and J-lead for surface mount packages, and straight form for through-hole mounting. During the forming process, extreme care is taken to avoid excessive abrasion to the solder, exposed base metal, scratches and solder flakes. Lead forming tool maintenance is critical to ensure good lead quality.

Figure 3-12. Formation of Gull-Wing Leads

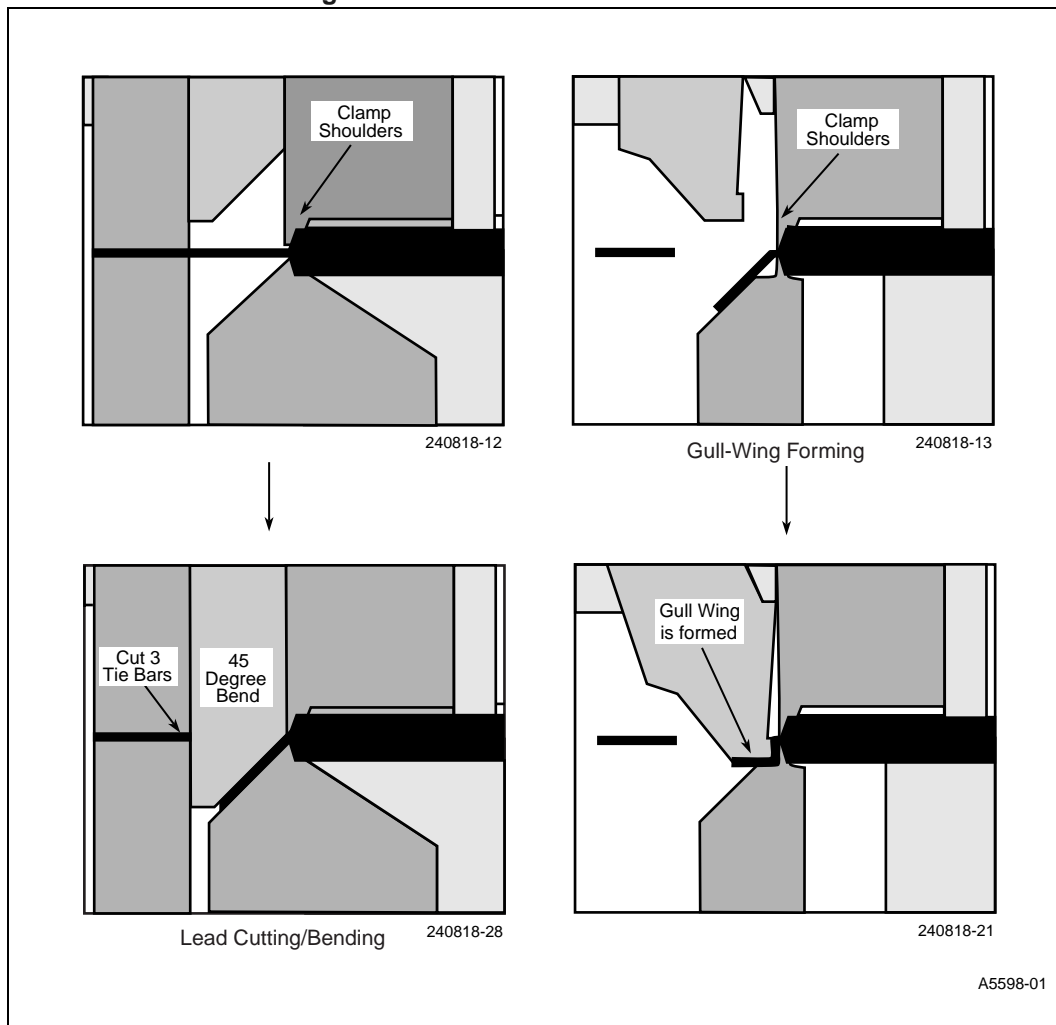


Figure 3-13. Formation of Gull-Wing Leads (continued)

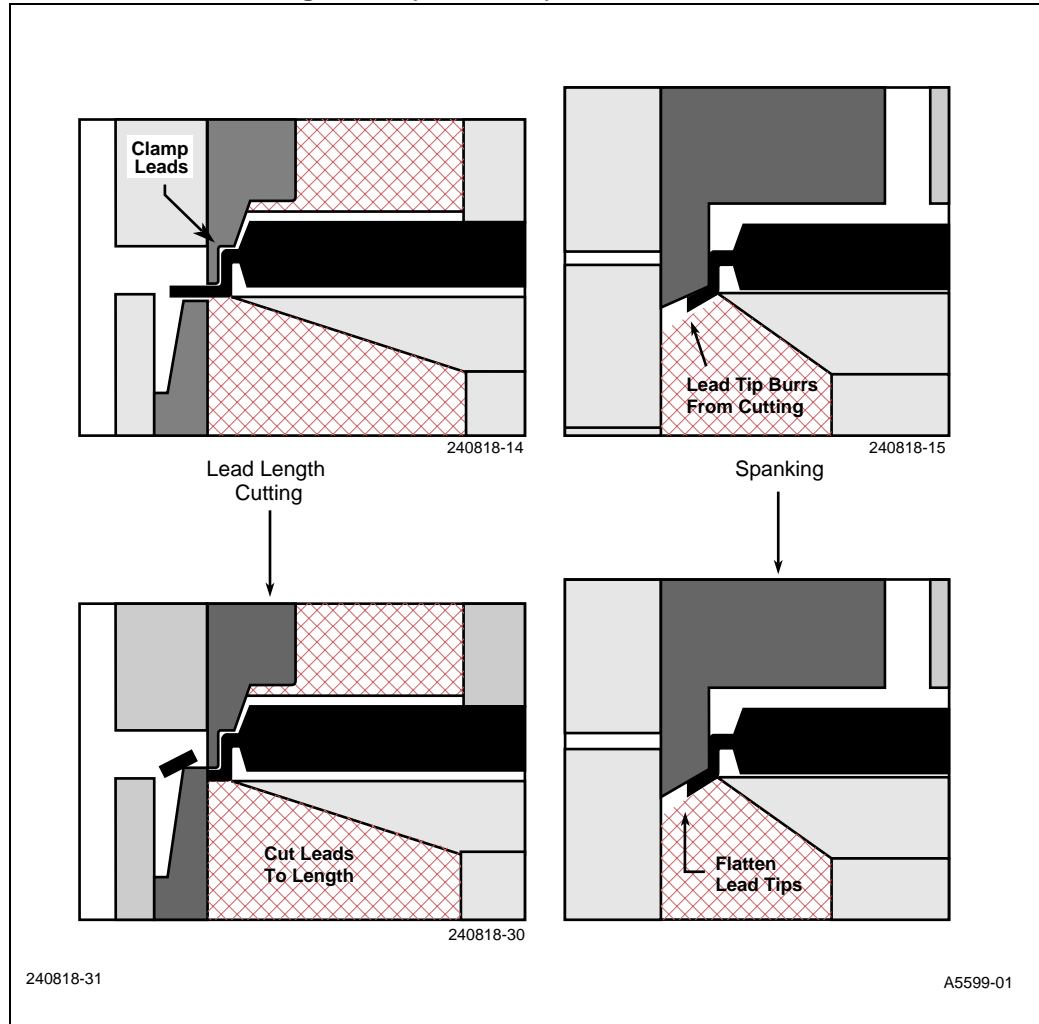
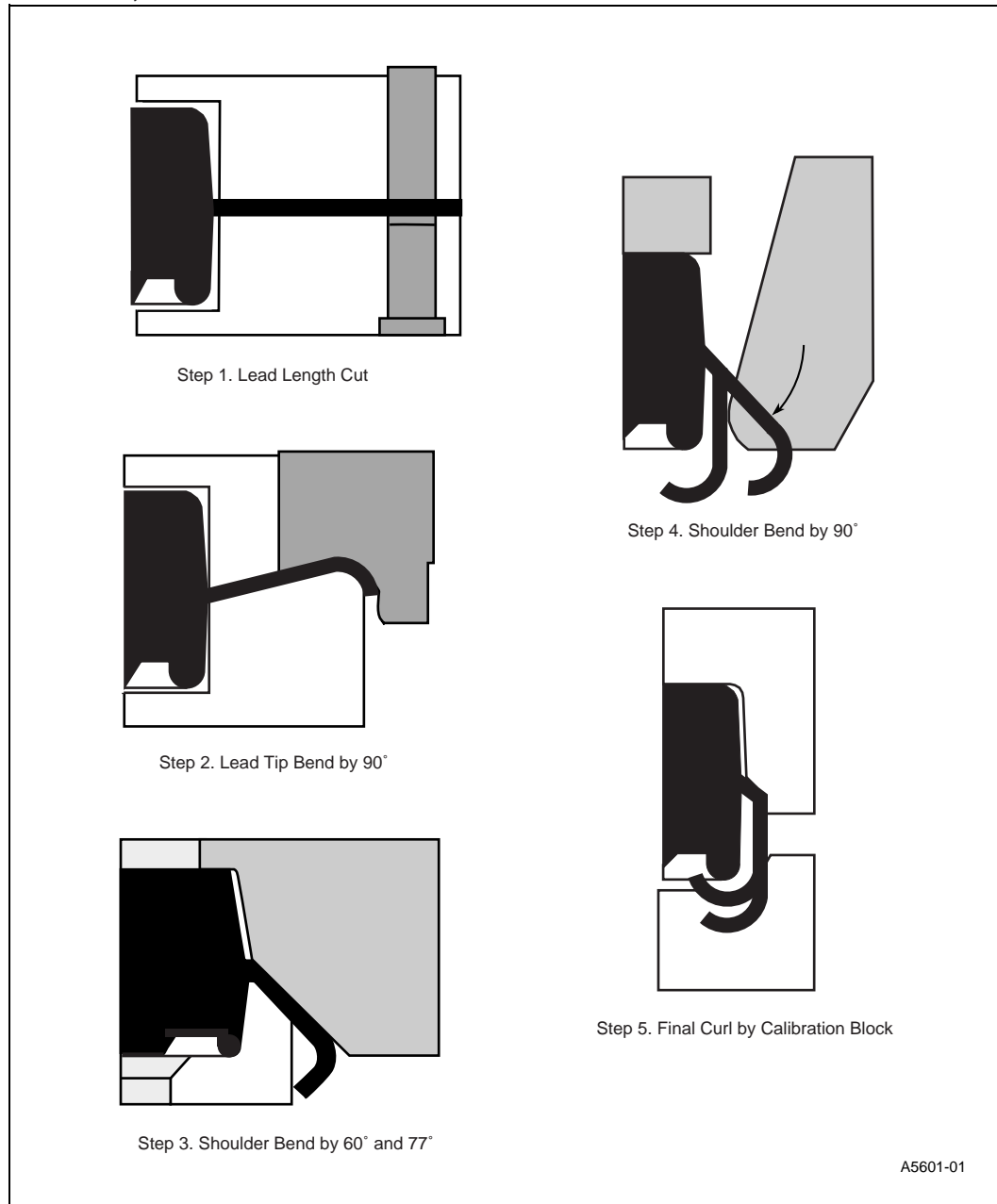


Figure 3-14. Deflash, Trim and Form of J-Leads on PLCCs



As part of the lead-forming process, dambars and excess molding compound or flash that has flowed between the leads and out to the dambars are removed simultaneously from the leads. This step electrically isolates the leads. Dambar removal and lead forming processes can either be done on two separate machines or an integrated machine.

Finally, individual units are separated or singulated from the lead frame and carefully transferred into tubes or trays before being sent to the testing process. These transport media such as tubes and trays are designed to protect the leads.

3.7 Hermetic Sealing

3.7.1 Packaging Options

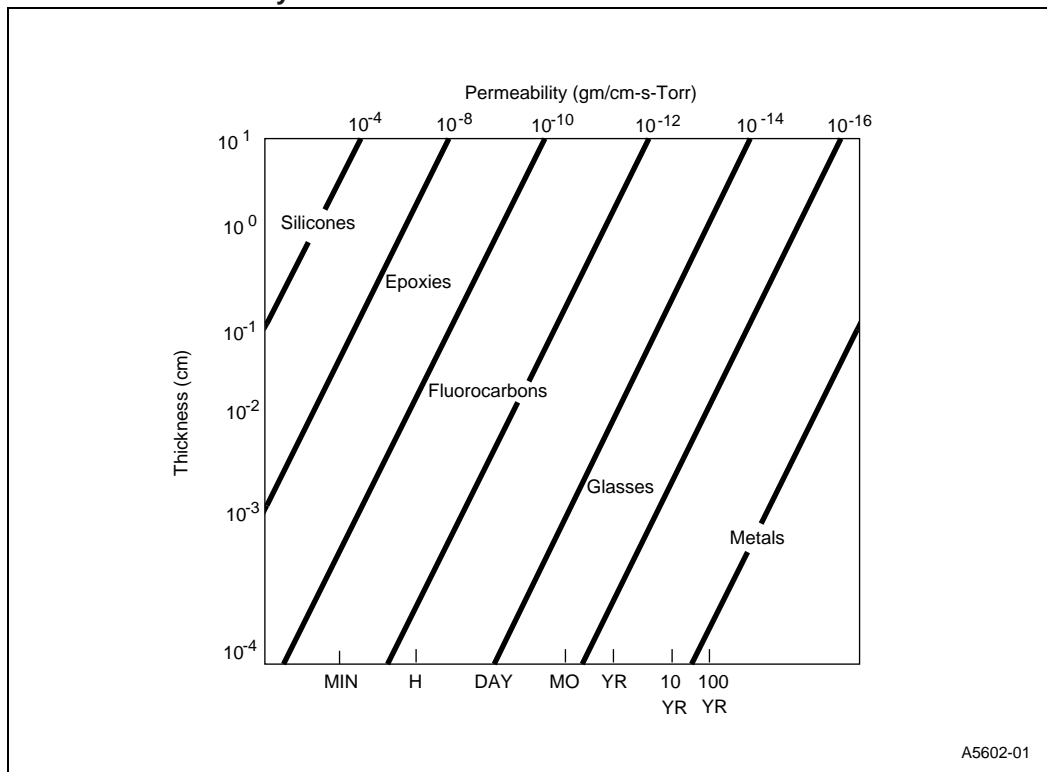
Hermetic sealing of IC packages is used to seal the die from the external environment, specifically from water vapor and contaminants that can shorten the lifetime of a sensitive electronic device.

Three types of hermetic seals are:

- precious metal eutectic alloy reflow (laminated ceramic package family),
- soft solder metal alloy reflow (laminated ceramic package family), and
- low melting-temperature glasses (pressed ceramic package family).

The precious metal eutectic alloy-sealed packages and soft solder metal alloy-sealed packages are of the laminated ceramic type. The precious metal eutectic alloy-sealed packages involve the brazing of a metal lid to a gold-plated thick-film seal ring on the ceramic. The second method uses soft solder metal alloy to fuse a ceramic lid to the seal ring of the ceramic package. The glass-sealed packages utilize glass to create the seal between pressed ceramic pieceparts. Figure 3-15 illustrates the relative hermeticity of various sealing materials. It can be seen from the graph that a metal seal provides the highest level of hermeticity, followed by glass and ceramic seals.

Figure 3-15. Relative Hermeticity of Materials



3.7.2 Materials

3.7.2.1 Laminated Ceramic Package Sealing

Two metal-sealed methods are: (1) precious metal eutectic alloy reflow; (2) soft solder metal alloy reflow.

3.7.2.2 Precious Metal Eutectic Alloy ReFlow (Metal Lid)

The precious metal eutectic reflow process utilizes a gold-tin eutectic hard solder to create the hermetic seal. Alloy composition is 80% gold, 20% tin, and has a melting point of 280°C (see Figure 3-16). This solder has excellent wetting characteristics to the seal ring and lid materials, and high resistance to thermal fatigue. Seals created by the Au-Sn alloy can withstand condition C (-65°C -150°C) thermal cycles.

Figure 3-16. Au-Sn Phase Diagram

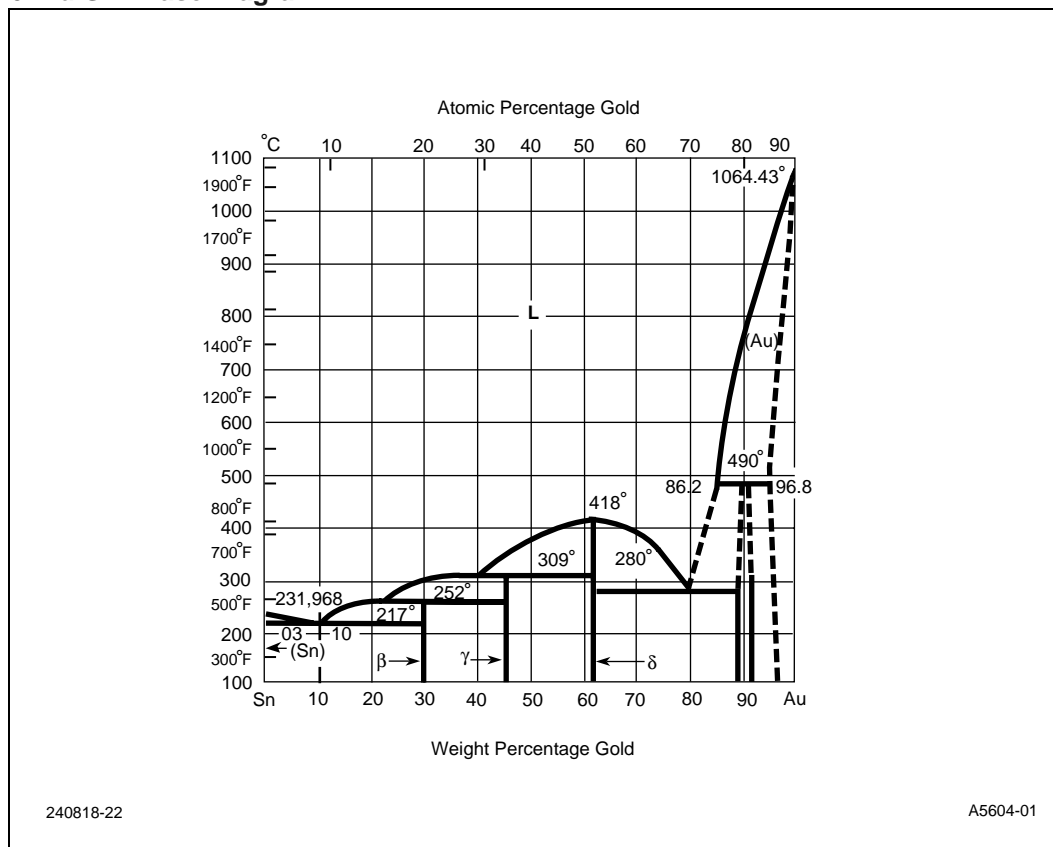
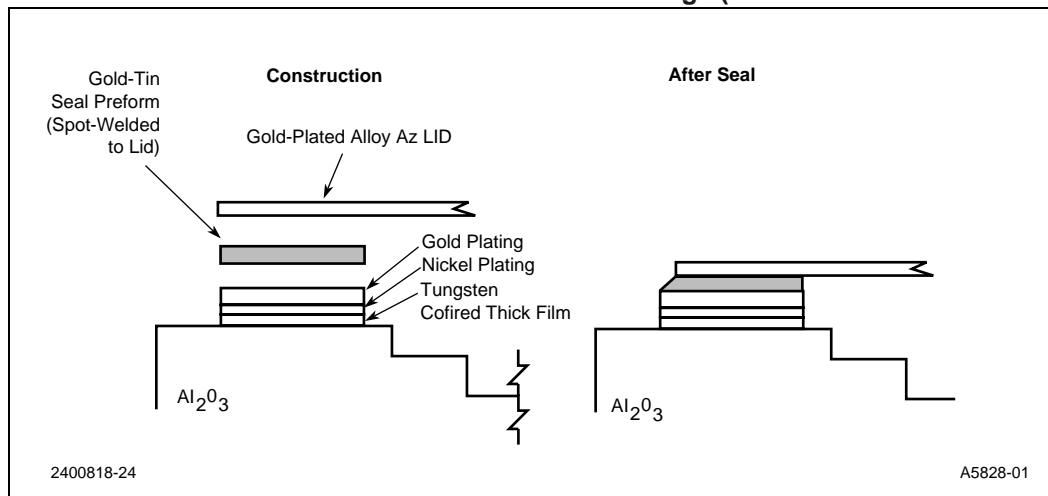


Figure 3-17. Schematic Cross-Section of a Metal Lid Seal Package (Thicknesses Not to Scale)



The gold-tin eutectic seal is made to a seal ring on the surface of the alumina ceramic. The seal ring is composed of a tungsten thick film that is co-fired to the ceramic material and plated with a thin nickel diffusion barrier and gold overplate. The gold overplate prevents oxidation and provides a wettable surface for the solder. Figure 3-17 is a schematic of the seal area.

The lid material is gold-plated Alloy 42 (a nickel-iron alloy with low thermal expansion) to which is attached an 80% gold, 20% tin alloy (eutectic composition) preform. The seal preform is attached by spot welding. The lid material was chosen for its stiffness and because the thermal expansion of Alloy 42 is quite close to that of aluminum oxide ceramic. The stiffness prevents damage during testing, and the low coefficient of thermal expansion (CTE) difference minimizes stress at the seal due to thermal expansion mismatch.

The gold thickness of the plating used in the seal ring area is important to the success of sealing this system. Gold thickness must be controlled to prevent premature nickel diffusion and oxidation at the gold surface, which can create a poorly wetted surface that will result in seal defects. The nickel diffusion barrier prevents the interdiffusion of tungsten and gold that can also result in seal defects.

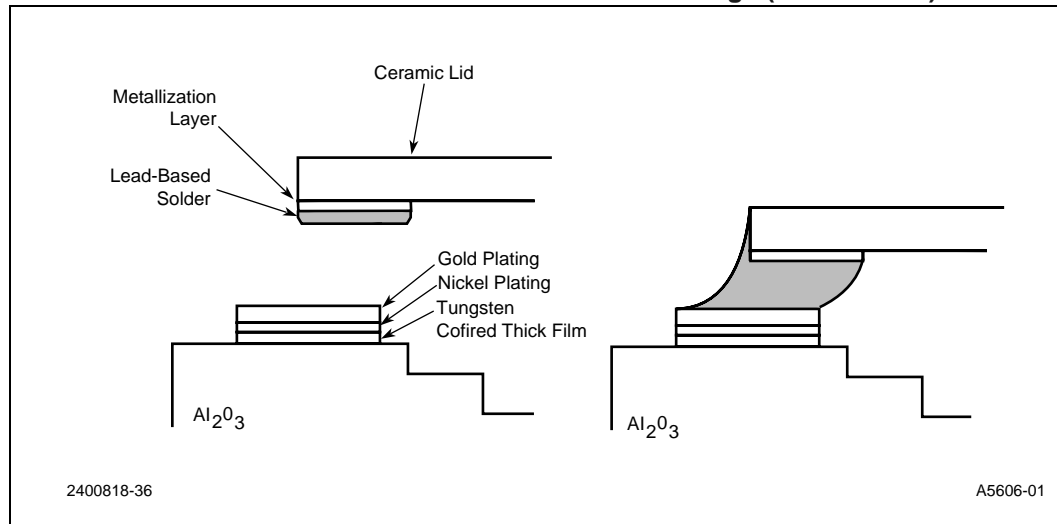
The seal preform width and thickness are also specified and controlled to ensure that an adequate amount of solder is present to create a continuous seal.

3.7.2.3 Soft Solder Alloy Reflow (Ceramic Lid)

The soft solder alloy reflow method is similar to the precious metal eutectic alloy reflow method with the exception of the lid and sealant material. It involves the fusing of a ceramic lid onto the ceramic package using a five-element lead-based soft solder. In this method the lid and package are of the same material thus minimizing thermal mismatch which can pose a reliability concern to bigger IC packages. Figure 3-18 is a schematic cross-section of a ceramic lid seal package.

The sealing process takes place in a forming gas environment which removes oxides from the sealant surface. Oxides, when present, inhibit solder flow and cause non-wetting which results in a non-hermetic seal. The pattern and solder dimensions are optimized to ensure maximum seal quality and reliability performance.

Figure 3-18. Schematic Cross-Section of a Ceramic Lid Seal Package (Not to Scale)



3.7.2.4 Glass-sealed Pressed Ceramic Packages

In glass-sealed packages, a ceramic lid is sealed to the base ceramic with a vitreous (noncrystallizing), lead-based glass having a low melting temperature. The glasses chosen for hermetic sealing are lead-zinc borates that generally seal in the 415-450° C range. Figure 3-20 illustrates the vitreous glass-forming region (region A) in the lead-zinc-borate system from which these glasses are chosen. The glasses used in the industry have composition in this range, with the final selection based on obtaining the lowest possible processing temperature. As a result, the most commonly available seal glasses have very similar compositions. The glasses are highly resistant to chemical plating baths (see Table 3-4) and have excellent thermal shock resistance.

Figure 3-19. Lead-Zinc-Borate Phase Diagram

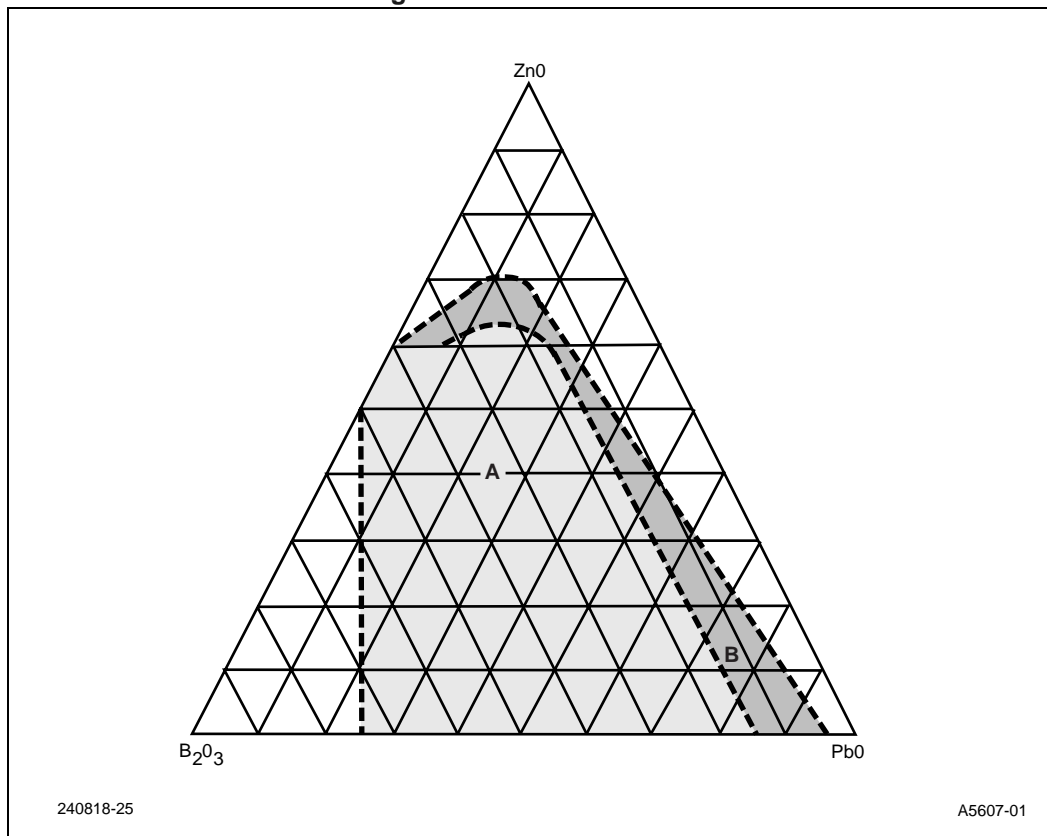


Table 3-4. Chemical Durability of Glasses Weight Loss (mg/cm²/hr)

Chemical Treatment	Glass Type			
	Intel	B	C	D
50% H ₂ SO ₄ , 95° C, 1 hr.	8.65	2.32	5.89	0.88
50% H ₂ SO ₄ , 25% HNO ₃ , 25° C	28.44	25.44	25.32	18.00
5% HNO ₃ , 25° C, Direct Transfer to 50% H ₂ SO ₄ at 95° C	323.60	385.60	226.80	250.80

NOTE: Glasses must exhibit chemical durability to withstand the lead-plating baths.

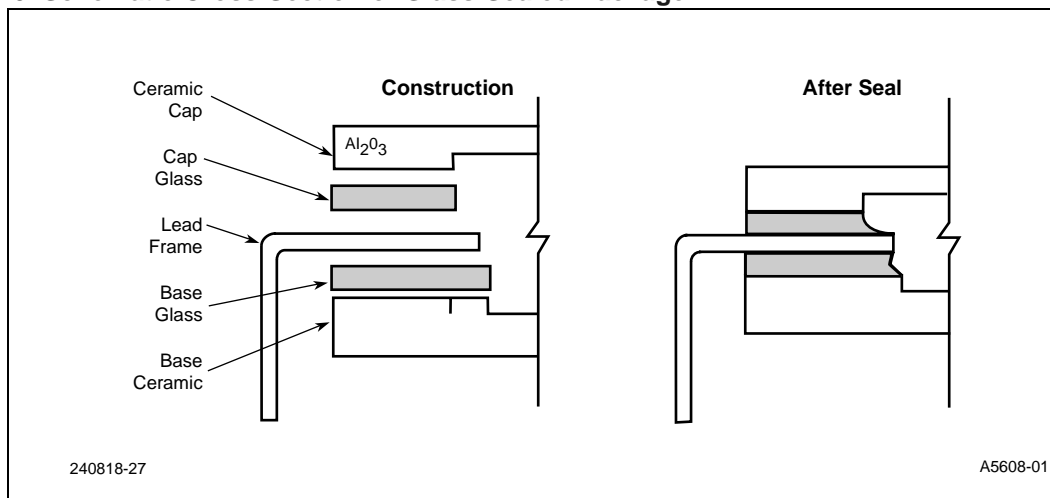
The glasses used for package sealing have high thermal expansions relative to the ceramic. To reduce thermally induced package stresses, it is necessary to reduce the thermal expansion of the glasses by adding low-thermal-expansion fillers. These fillers are chosen to be compatible with the lead glass and do not react during processing.

Because the glasses have similar compositions, they have similar strengths. Table 3-5 lists the measured bending strengths for several different sealing glasses commonly used. The glass used by Intel can be seen to have bending strengths equivalent to other commonly used glasses. The fracture toughness of Intel's sealing glass is also found to be quite similar. It is expected that the mechanical performance of Intel's sealing glass will be equivalent to other commonly used glasses.

Table 3-5. Bending Strengths and Fracture Toughness of Several Lead-Based Sealing Glasses

Glass	Four Point Bending Strength (MPa)	Fracture Toughness (MPa \sqrt{m})
Intel	20.1	1.0
B	21.4	1.1
C	20.0	0.9

Figure 3-20. Schematic Cross-Section of Glass-Sealed Package



3.7.3 Processes

3.7.3.1 Laminated Ceramic Processing

Sealing of metal-sealed packages is accomplished in a continuous belt furnace. The metal lid is centered and clipped in place to ensure that the seal ring and preform remain properly aligned and that sufficient pressure is exerted on the lid to provide good contact. The units are elevated in temperature past the melting temperature of the alloy and allowed to soak at the sealing temperature. The soak period allows the molten metal time to wet all the sealing surfaces sufficiently and to form an integral metallurgical bond with the seal ring and lid plating.

Sealing can be accomplished in either an inert (nitrogen) or reducing atmosphere (forming gas N_2H_2). The seals obtained with either atmosphere are equivalent in performance. The reducing atmosphere is used to build additional margin into the sealing process.

The sealing process is controlled by monitoring the seal temperatures with a thermocouple embedded in a package that is passed through a fully loaded furnace. This ensures that the furnace profile obtained is representative of that seen by actual product. Water vapor content of the sealing atmosphere is also controlled to ensure that the final internal-cavity water vapor levels meet industry requirements.

3.7.3.2 Pressed Ceramic Processing

Glass-sealed packages are sealed in a continuous dry air atmosphere belt furnace. Caps and bases are held in fixtures during the seal process to provide proper alignment of the top and bottom of the package. No clips are used; the package weight is sufficient to create the seal. Because glass does not have a sharp melting point, it is necessary to hold the units at the seal temperature for sufficient time to allow glass flow and wet the metal lead frame and ceramic, thus creating the final seal. Insufficient time will result in noncontinuous seals or incomplete flow, causing glass depressions between the leads. These depressions in their worst form can create a continuous path to the cavity (non-hermetic), or in less severe cases act as a stress riser and result in package damage during subsequent handling. Sealing is performed in an oxidizing ambient (dry air) to prevent reduction of the lead glass.

As with the metal-sealed packages, the process is controlled by profiling a fully loaded furnace by means of a thermocouple embedded in a CERDIP-type package, to get an accurate representation of the actual sealing conditions. Water vapor content and flow rates of the atmosphere are controlled to ensure that the internal-cavity water vapor requirements are met.

3.7.4 Performance

Intel's hermetic packages can be tested for hermeticity using two tests: fine and gross leak. Two tests are required, since neither test can adequately detect the entire range of leak sizes. Fine leak uses helium and a mass spectrograph to identify fine leaks. Larger leaks do not show up, as the gases leak out too quickly for the detectors to identify. The industry-acceptable leak rate for hermetic packages is less than 5×10^{-8} Std. CC atm/min.

Gross leak testing, which identifies larger leaks that fine leak testing cannot detect, employs a high-vapor pressure fluorocarbon liquid as the detection medium. The unit is pressurized in a container of the fluorocarbon to force the liquid into potential leakage paths. After pressurization, the unit is immersed in a hot bath, which vaporizes the fluorocarbon trapped in the leak. A steady stream of bubbles indicates the location of the leak. The gross leak test cannot be used for small leaks, as the liquid will not penetrate leaks smaller than a certain size.

3.8 Revision Summary

- General review & update of all sections

