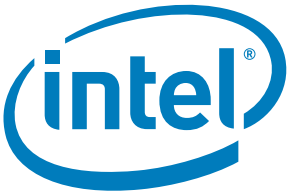

PCIe* 5.0 Retimer Supplemental Features and Standard BGA Footprint

Specification

Revision 1.0

April 2022

Reference Number: 619169

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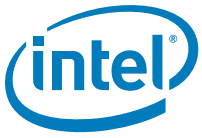


Tables

Revision History

Document Number	Revision Number	Description	Date.
619169	0.3	• Initial Release of the PCIe Gen5 Retimer Footprint Specification. Pinout proposed same as Gen4. • Added note #3 to Table 1-2. • Added implementation note emphasizing importance of PTH vias next to outer periphery GND pins. • Updated Table 4.1.	August 2018
619169	0.5	• Added pin locations for x16 Power Pins and added an Annex section listing x16 GND pins • Updated supported power rails, removed support for 3.3 V and 0.8 V. • Updated the register configuration section to add Interrupt, Status and mask registers. • Updated the register configuration offset table.	February 2019
619169	0.7	• Added Description column to the register configuration Table. • Corrected SMBus examples. • Added pin list in the Annex section. • Added clarification on supported clocking architectures. • Updated PWR_1 and PWR_2 rails to VD_PWR. • Added Reset Register to the list of defined registers.	January 2020
619169	0.71	• Added Base spec inband address mapping table. • Removed 3.3 V tolerant requirement from JTAG signals. • Correct package side pinout for x8 retimer.	September 2020
619169	0.9	• Added Host Defined register 3 in section 6.21. • Added Host Defined register 4 in section 6.21.	November 2021
619169	1.0	• Updated Version to 1.0 release.	April 2022

§

1 Introduction

1.1 Overview

PCI Express* (PCIe*) 5.0 capable retimers extend the channel reach on a platform to beyond what is possible otherwise.

With PCIe 5.0 (32 GT/s), the data rate has increased by 2x compared to the previous generation (16 GT/s), resulting in an even shorter channel reach compared to 16GT/s.

Common use cases include channels expanding over system boards, backplanes, cables, risers, and Add-in Cards. Such long channels can have losses that far exceeds the specification loss target of -36 dB at 16 GHz. Retimers have been part of PCIe 4.0/ 5.0 base specification. PCI-SIG is expected to implement a compliance program for testing retimers.

It is expected that the majority of the platforms using PCIe 5.0 will require retimers. Multiple sources of retimers will make the adoption of PCIe 5.0 technology easier. Common footprint simplifies the platform design process. The pinout is optimized for 32 GT/s, and a 16 GT/s signal integrity and thermal challenges.

Figure 1-1 through Figure 1-4 show a few example configurations involving the Riser, Mother Board and Add-in Card. Various other configurations are possible.

Figure 1-1. Platform Configuration with an Add-in Card and Retimer on Mother Board

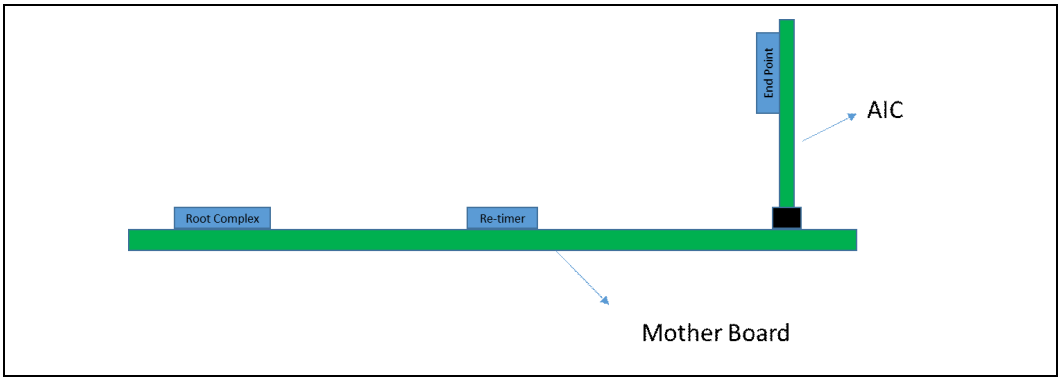


Figure 1-2. Platform Configuration with an Add-in Card and Riser, Retimer on Riser

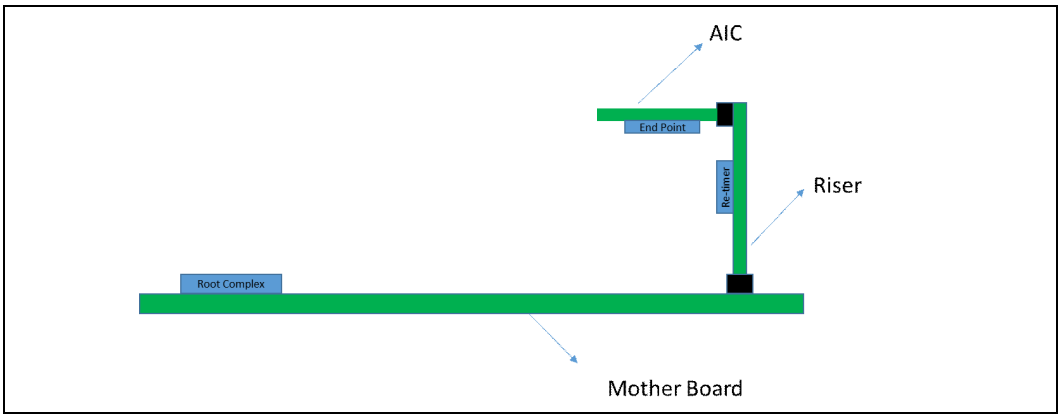


Figure 1-3. Platform Configuration with a Riser and Cable, Retimer is on Riser

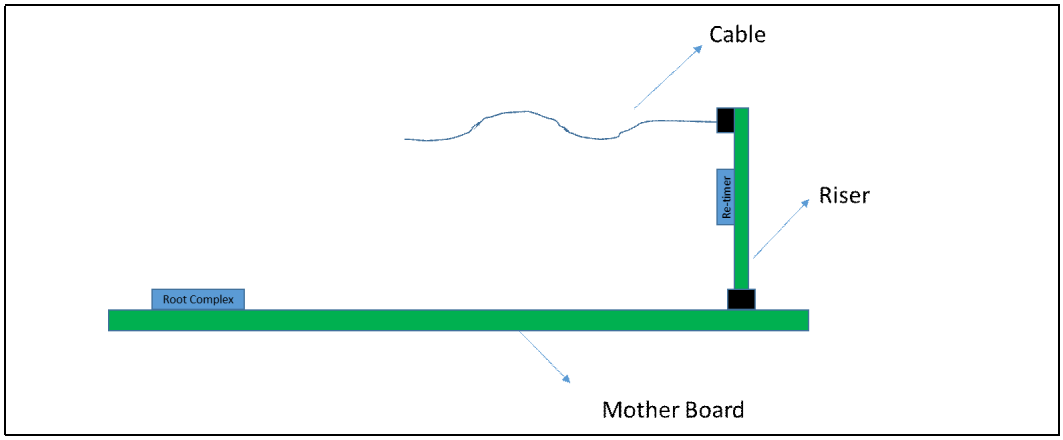
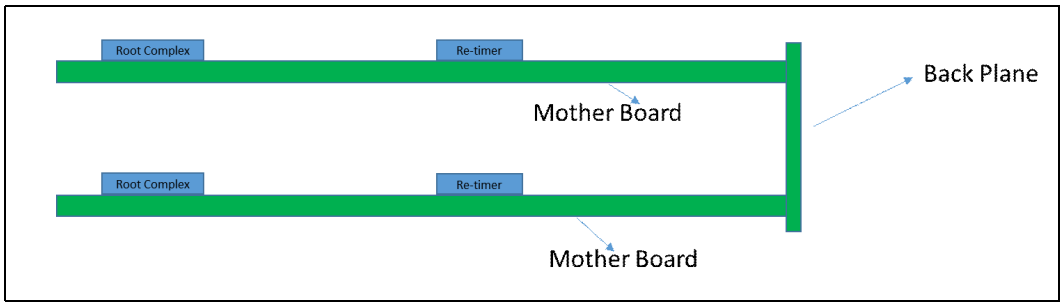


Figure 1-4. Platform Configuration with a Backplane, Retimer on both Mother Boards



1.2 Terminology

The "#" symbol at the end of a signal name indicates that the Active or Asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when the signal is at a high voltage level.

The following notations are used to describe the various signal types:

Table 1-1. Abbreviations

Term	Description
I	Input
O	Output
I/O	Bi-Directional
PTH	Plated Through Hole
PU	Pull-up
PWR	Power
GND	Ground
Host	This term is synonymous with platform or system
NC	No Connect
VD	Vendor Defined
SSC	Spread Spectrum Clocking
SRIS	Separate Reference Clock Independent SSC

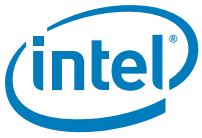


Table 1-1. Abbreviations

Term	Description
RX	PCIe Receiver
TX	PCIe Transmitter
N/A	Not Applicable

1.3 Specification References

This specification requires references to other specifications or documents that will form the basis for some of the requirements stated herein.

- PCI Express Card Electromechanical (CEM) Specification, Revision 5.0, Version 0.5.
- PCI Express Base Specification, Revision 5.0, Version 1.0.
- System Management Bus (SMBus) Specification, Version 2.0, August 3, 2000.
- JTAG Specification (IEEE 1149.1).
- I2C BUS Specifications, Version 2.1, January 2000.

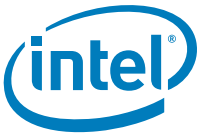
1.4 Retimer Supplemental Features Beyond PCIe 5.0 Base Specification

Table 1-2 lists the features that are either optional or not specified for retimers in the PCIe Base Specification, but are required for the retimers following this specification.

Table 1-2. Retimer Feature Comparison

Feature	PCIe 5.0 Base Specification for Retimers	PCIe 5.0 for Retimers, Supplemental Features and Standard BGA Footprint Specification
SRIS	Optional	Required
Slave Loopback	Optional	Required
Receiver Lane Margining (Voltage)	Optional	Required
Link Subdivision (Bifurcation)	Not defined explicitly, but can be supported	Required
L1PM Substates[1]	Optional	Required[2]
SMBus Programmable Configurations	N/A	Required
Support for EEPROM load configuration	N/A	Optional
Retimer Common (size, pinout) Footprint	N/A	Required
Reference Clock Out	N/A	Required

Notes:
1. L1PM Substate support for retimers as defined in the PCIe Base Specification.
2. If the platform does not support L1 PM Substates, it may not drive/route the CLKREQ# to the Retimer; in that case, the Retimer must take care of pulling the CLKREQ# pin low using an implementation specific manner.



1.4.1 Link Subdivision

Link subdivision (also known as bifurcation) is the division of a PCIe Link into a number of independent links. Each of the subdivided links behave as an independent PCIe link, and is required to follow the PCIe Link requirements. For example, each of these subdivided links should support defaulting to x1 Link width if the link can't be trained at the required link width. Each subdivided link is completely independent and can operate at different link speeds.

The *Global Parameter* register in the Retimer is updated with the required link subdivision using SMBus commands. If the Retimer is on the mother board, the mother board can update the register with the required configuration; or if the Retimer is on a Riser, the Riser can take care of knowing what configuration the end points need and then updating the register in the Retimer accordingly.

A Host is required to issue a warm reset to the Retimer to retrain the link with updated link subdivision settings.

All of the subdivided sub-links are required to operate in Common REF CLK mode, SRIS or SRNS mode. Having some subdivided links operating in common REFCLK configuration and some operating in Separate REF CLK mode is not supported at this time, due to pin limitations on the Retimer.

1.4.2 Retimer Clocking

When the Retimer is operating in the Common Clock mode, it is required to replicate the clock it receives on its REFCLK pins onto the REFCLK_Out pins. For example, if the incoming REFCLK has SSC, the clock that the Retimer outputs on the RFECLK_Out pins is required have SSC; if the incoming REFCLK does not have SSC enabled, the clock that the Retimer outputs on the RFECLK_Out pins is required to have SSC disabled.

When the Retimer is configured in SRIS or SRNS mode, it replicates the clock it receives on REFCLK pins, onto its REFCLK_Out pins. The clock that the Retimer sees on its REFCLK pins will be the clock that is locally generated for the Retimer when Retimer is not located on the motherboard. This locally generated clock will have SSC enabled when the Retimer is configured in SRIS mode, and will have SSC disabled when the Retimer is configured in SRNS mode.

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2 Mechanical Specification

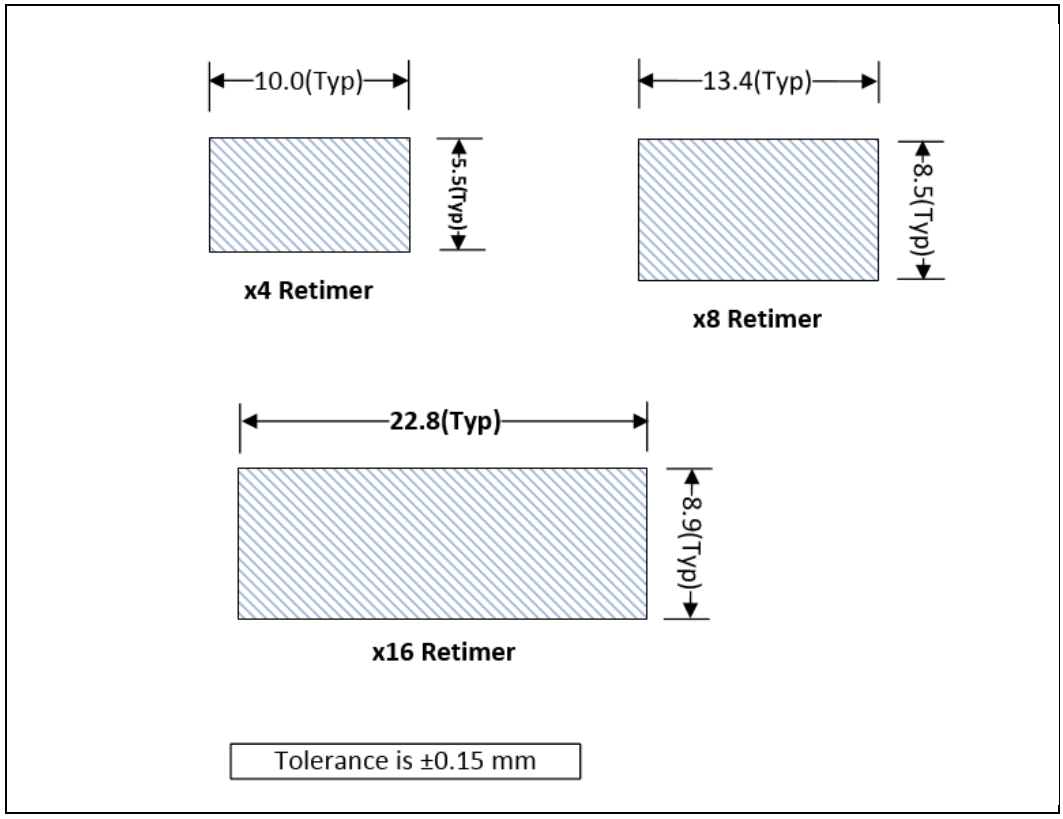
2.1 Overview

Three different retimer package sizes are specified:

- x4: Supports 4 lanes in upstream direction and 4 lanes in downstream direction.
- x8: Supports 8 lanes in upstream direction and 8 lanes in downstream direction.
- x16: Supports 16 lanes in upstream direction and 16 lanes in downstream direction.

Figure 2-1 shows the overall package dimensions for the three retimer form factors. Note that all the dimensions are in millimeters (mm) and the tolerance is ±0.15 mm.

Figure 2-1. Retimer Form Factors



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3 Signal Description

This chapter provides a detailed description of retimer signals. The signal descriptions are arranged in functional groups according to their associated interface.

Signal directions in Table 3-1, Table 3-2 and Table 3-3 are from the retimer perspective. In these cases, "O" indicates output from the retimer device, and "I" indicates input to the retimer device.

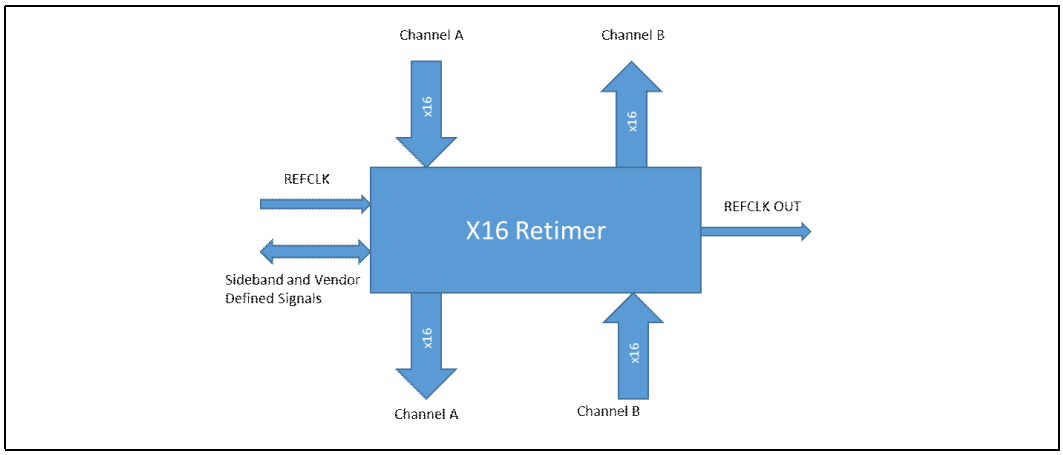
Signals labeled "VD" are Vendor Defined. It is required that VD balls carry signals that are not critical to retimer basic functionality and are used for providing enhanced or debug features.

Common footprint for following link widths are defined for the PCIe 5.0 retimers:

1. x16 (Link with 16 physical lanes)
2. x8 (Link with 8 physical lanes)
3. x4 (Link with 4 physical lanes)

Figure 3-1 shows the x16 retimer block diagram. Channel A and Channel B are ports that can be configured to be upstream or downstream.

Figure 3-1. x16 Retimer Block Diagram



3.1 Retimer Interface Signals

Table 3-1 lists the pin numbers and functions for each of the pins in x16 pinout, along with voltage level whenever applicable.

Table 3-1. Retimer Signal Descriptions

Pin	Signal Name	Signal Direction	Signal Description	Voltage Level
High Speed Differential I/O				
M26	A_PETp0	O	Transmitter differential pair, A Channels, Lane 0	
P29	A_PETn0	O		

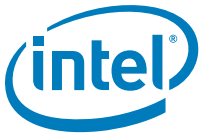


Table 3-1. Retimer Signal Descriptions (Continued)

Pin	Signal Name	Signal Direction	Signal Description	Voltage Level
W26	A_PETp1	O	Transmitter differential pair, A Channels, Lane 1	
AA29	A_PETn1	O		
AF26	A_PETp2	O	Transmitter differential pair, A Channels, Lane 2	
AH29	A_PETn2	O		
AN26	A_PETp3	O	Transmitter differential pair, A Channels, Lane 3	
AR29	A_PETn3	O		
AY26	A_PETp4	O	Transmitter differential pair, A Channels, Lane 4	
BB29	A_PETn4	O		
BG26	A_PETp5	O	Transmitter differential pair, A Channels, Lane 5	
BJ29	A_PETn5	O		
BP26	A_PETp6	O	Transmitter differential pair, A Channels, Lane 6	
BT29	A_PETn6	O		
CA26	A_PETp7	O	Transmitter differential pair, A Channels, Lane 7	
CC29	A_PETn7	O		
CH26	A_PETp8	O	Transmitter differential pair, A Channels, Lane 8	
CK29	A_PETn8	O		
CR26	A_PETp9	O	Transmitter differential pair, A Channels, Lane 9	
CU29	A_PETn9	O		
DB26	A_PETp10	O	Transmitter differential pair, A Channels, Lane 10	
DD29	A_PETn10	O		
DJ26	A_PETp11	O	Transmitter differential pair, A Channels, Lane 11	
DL29	A_PETn11	O		
DT26	A_PETp12	O	Transmitter differential pair, A Channels, Lane 12	
DV29	A_PETn12	O		
EC26	A_PETp13	O	Transmitter differential pair, A Channels, Lane 13	
EE29	A_PETn13	O		
EK26	A_PETp14	O	Transmitter differential pair, A Channels, Lane 14	
EM29	A_PETn14	O		
EU26	A_PETp15	O	Transmitter differential pair, A Channels, Lane 15	
EW29	A_PETn15	O		
N34	B_PERp0	I	Receiver differential pair, B Channels, Lane 0	
R35	B_PERn0	I		
Y34	B_PERp1	I	Receiver differential pair, B Channels, Lane 1	
AB35	B_PERn1	I		
AG34	B_PERp2	I	Receiver differential pair, B Channels, Lane 2	
AJ35	B_PERn2	I		
AP34	B_PERp3	I	Receiver differential pair, B Channels, Lane 3	
AT35	B_PERn3	I		
BA34	B_PERp4	I	Receiver differential pair, B Channels, Lane 4	
BC35	B_PERn4	I		

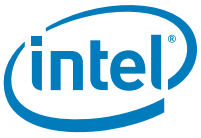


Table 3-1. Retimer Signal Descriptions (Continued)

Pin	Signal Name	Signal Direction	Signal Description	Voltage Level
BH34	B_PERp5	I	Receiver differential pair, B Channels, Lane 5	
BK35	B_PERn5	I		
BR34	B_PERp6	I	Receiver differential pair, B Channels, Lane 6	
BU35	B_PERn6	I		
CB34	B_PERp7	I	Receiver differential pair, B Channels, Lane 7	
CD35	B_PERn7	I		
CJ34	B_PERp8	I	Receiver differential pair, B Channels, Lane 8	
CL35	B_PERn8	I		
CT34	B_PERp9	I	Receiver differential pair, B Channels, Lane 9	
CV35	B_PERn9	I		
DC34	B_PERp10	I	Receiver differential pair, B Channels, Lane 10	
DE35	B_PERn10	I		
DK34	B_PERp11	I	Receiver differential pair, B Channels, Lane 11	
DM35	B_PERn11	I		
DU34	B_PERp12	I	Receiver differential pair, B Channels, Lane 12	
DW35	B_PERn12	I		
ED34	B_PERp13	I	Receiver differential pair, B Channels, Lane 13	
EF35	B_PERn13	I		
EL34	B_PERp14	I	Receiver differential pair, B Channels, Lane 14	
EN35	B_PERn14	I		
EV34	B_PERp15	I	Receiver differential pair, B Channels, Lane 15	
EY35	B_PERn15	I		
R1	A_PERp0	I	Receiver differential pair, A Channels, Lane 0	
N2	A_PERn0	I		
AB1	A_PERp1	I	Receiver differential pair, A Channels, Lane 1	
Y2	A_PERn1	I		
AJ1	A_PERp2	I	Receiver differential pair, A Channels, Lane 2	
AG2	A_PERn2	I		
AT1	A_PERp3	I	Receiver differential pair, A Channels, Lane 3	
AP2	A_PERn3	I		
BC1	A_PERp4	I	Receiver differential pair, A Channels, Lane 4	
BA2	A_PERn4	I		
BK1	A_PERp5	I	Receiver differential pair, A Channels, Lane 5	
BH2	A_PERn5	I		
BU1	A_PERp6	I	Receiver differential pair, A Channels, Lane 6	
BR2	A_PERn6	I		
CD1	A_PERp7	I	Receiver differential pair, A Channels, Lane 7	
CB2	A_PERn7	I		
CL1	A_PERp8	I	Receiver differential pair, A Channels, Lane 8	
CJ2	A_PERn8	I		

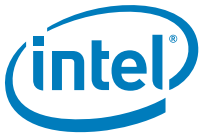


Table 3-1. Retimer Signal Descriptions (Continued)

Pin	Signal Name	Signal Direction	Signal Description	Voltage Level
CV1	A_PERp9	I	Receiver differential pair, A Channels, Lane 9	
CT2	A_PERn9	I		
DE1	A_PERp10	I	Receiver differential pair, A Channels, Lane 10	
DC2	A_PERn10	I		
DM1	A_PERp11	I	Receiver differential pair, A Channels, Lane 11	
DK2	A_PERn11	I		
DW1	A_PERp12	I	Receiver differential pair, A Channels, Lane 12	
DU2	A_PERn12	I		
EF1	A_PERp13	I	Receiver differential pair, A Channels, Lane 13	
ED2	A_PERn13	I		
EN1	A_PERp14	I	Receiver differential pair, A Channels, Lane 14	
EL2	A_PERn14	I		
EY1	A_PERp15	I	Receiver differential pair, A Channels, Lane 15	
EV2	A_PERn15	I		
M7	B_PETp0	O	Transmitter differential pair, B Channels, Lane 0	
P10	B_PETn0	O		
W7	B_PETp1	O	Transmitter differential pair, B Channels, Lane 1	
AA10	B_PETn1	O		
AF7	B_PETp2	O	Transmitter differential pair, B Channels, Lane 2	
AH10	B_PETn2	O		
AN7	B_PETp3	O	Transmitter differential pair, B Channels, Lane 3	
AR10	B_PETn3	O		
AY7	B_PETp4	O	Transmitter differential pair, B Channels, Lane 4	
BB10	B_PETn4	O		
BG7	B_PETp5	O	Transmitter differential pair, B Channels, Lane 5	
BJ10	B_PETn5	O		
BP7	B_PETp6	O	Transmitter differential pair, B Channels, Lane 6	
BT10	B_PETn6	O		
CA7	B_PETp7	O	Transmitter differential pair, B Channels, Lane 7	
CC10	B_PETn7	O		
CH7	B_PETp8	O	Transmitter differential pair, B Channels, Lane 8	
CK10	B_PETn8	O		
CR7	B_PETp9	O	Transmitter differential pair, B Channels, Lane 9	
CU10	B_PETn9	O		
DB7	B_PETp10	O	Transmitter differential pair, B Channels, Lane 10	
DD10	B_PETn10	O		
DJ7	B_PETp11	O	Transmitter differential pair, B Channels, Lane 11	
DL10	B_PETn11	O		
DT7	B_PETp12	O	Transmitter differential pair, B Channels, Lane 12	
DV10	B_PETn12	O		

Table 3-1. Retimer Signal Descriptions (Continued)

Pin	Signal Name	Signal Direction	Signal Description	Voltage Level
EC7	B_PETp13	O	Transmitter differential pair, B Channels, Lane 13	
EE10	B_PETn13	O		
EK7	B_PETp14	O	Transmitter differential pair, B Channels, Lane 14	
EM10	B_PETn14	O		
EU7	B_PETp15	O	Transmitter differential pair, B Channels, Lane 15	
EW10	B_PETn15	O		
Reference Clock				
FJ16	REFCLK+	I	100 MHz. Reference Clock (Differential Pair) as defined by the PCIe Base Specification	
FF18	REFCLK-	I		
B16	REFCLK_Out+ [2]	O	100 MHz. This pin is used for driving REFCLK_out+	
E18	REFCLK_Out- [2]	O	100 MHz. This pin is used for driving REFCLK_Out-	
PCIe Auxiliary Signals				
F2	PERST#	I	Fundamental Reset; Active Low	1.8 V (3.3 V tolerant)
G35	CLKREQ#	I	Used by L1PM Substates; Active Low	1.8 V (3.3 V tolerant)
JTAG				
B6	JTAG_TDI	I	JTAG Test Data In	1.8 V
B9	JTAG_TDO	O	JTAG Test Data Out; Open drain; Requires pull up to 1.8V on the platform	
B12	JTAG_TMS	I	JTAG Test Mode Select	1.8 V
B3	JTAG_TCK	I	JTAG Clock	1.8 V
E8	JTAG_TRST#	I	JTAG Reset; Active Low	1.8 V
System Management Bus (SMBus)				
B31	SMBCLK	I/O	SMBus Clock Input / Open Drain Clock Output	1.8 V (3.3 V tolerant)
B28	SMBDAT	I/O	SMBus Data Input / Open Drain Output	1.8 V (3.3 V tolerant)
F34	SMB_ADDR_1	I	SMBus Address Bit1	1.8 V (3.3 V tolerant)
B23	SMB_ADDR_2	I	SMBus Address Bit2	1.8 V (3.3 V tolerant)
B25	SMB_ADDR_3 / VD_16 [1]	I	SMBus Address Bit3 or Vendor Defined	1.8 V (3.3 V tolerant)
EEPROM Configuration Interface				
FJ3	EE_DAT/ VD_7 [1]	I/O	EEPROM Interface Data or Vendor Defined	1.8 V (3.3 V tolerant)
FF5	EE_CLK/ VD_8 [1]	I/O	EEPROM Interface Clock or Vendor Defined	1.8 V (3.3 V tolerant)
Miscellaneous				
FJ23	VD_1 [1]	TBD	Vendor Defined Signal	
FF24	VD_2 [1]	TBD	Vendor Defined Signal	
FJ6	VD_3 [1]	TBD	Vendor Defined Signal	
FF8	VD_4 [1]	TBD	Vendor Defined Signal	

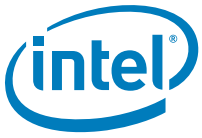


Table 3-1. Retimer Signal Descriptions (Continued)

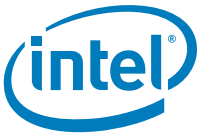
Pin	Signal Name	Signal Direction	Signal Description	Voltage Level
FJ9	VD_5[1]	TBD	Vendor Defined Signal	
FF11	VD_6[1]	TBD	Vendor Defined Signal	
FJ25	VD_9[1]	TBD	Vendor Defined Signal	
FF27	VD_10[1]	TBD	Vendor Defined Signal	
FJ28	VD_11[1]	TBD	Vendor Defined Signal	
FF30	VD_12[1]	TBD	Vendor Defined Signal	
FJ31	VD_13[1]	TBD	Vendor Defined Signal	
FF33	VD_14[1]	TBD	Vendor Defined Signal	
G1	VD_15[1]	TBD	Vendor Defined Signal	
E11	RX_DET_BYP	I	Receiver Detection Bypass	1.8 V (3.3 V tolerant)
FG1, FH2, FE2, D1, A1, C2, A35, D35, C34, FH34, FE34, FG35	NCTF		NCTF pins are **recommended** to be connected to Host ground, but are not **required** to connect to Host ground	GND or NC
Power				
30 pins CM17, CM20, CE17, CE20, BV17, BV20, EP17, EP20, EG17, EG20, DY17, DY20, DN17, DN20, DF17, DF20, CW17, CW20, BL17, BL20, BD17, BD20, AU17, AU20, AK17, AK20, AC17, AC20, T17, T20	VD_PWR		Vendor Defined Power- These balls are assigned for Power only. The actual voltage on specific balls and the tolerance are to be decided between the Platform Vendor and the Retimer Vendor.	
152 Pins[3]	GND		0 V	

Notes:
1. It is safe to route high speed Vendor Defined (VD) signals at these locations. Care must be taken to provide enough GND isolation. Retimer vendors are recommended to do a thorough signal integrity analysis when using any of the VD pins. Detailed SI analysis should be performed to decide whether unused VD pins can be left floating or need to be terminated or grounded on the platform side/Retimer side.
2. REFCLK Out is compliant with REFCLK definition in the PCIe Base Specification. Refer to Section 1.4.2, "Retimer Clocking" for additional details.
3. Refer to Section 7.1, "Pin List for x16 Pinout" for a complete list of x16 pins.

3.1.1 Signal Descriptions

3.1.1.1 SMBus Interface

SMBCLK, SMBDAT and three address pins (SMB_ADDR_1, SMB_ADDR_2, SMB_ADDR_3) are assigned in the ballmap. The three address bits are required to address retimers on the SMBus in a platform configuration. Retimer Vendors are allowed to take care of SMBus address needs on the platform by using only two address pins (SMB_ADDR_1, SMB_ADDR_2) if they can take care of additional addresses needed by the platform in a proprietary way. Retimer Vendors can use the third address pin for Vendor Defined purposes in that case. The address pin SMB_ADDR_3 can be used for Vendor Defined signal.



SMBus implementation is required to support 100 KHz, and be 400 KHz compatible.

3.1.1.2 EEPROM Interface

EECLK and EEDAT signals are defined to load the initial configuration from an external EEPROM. No specific interface is mentioned, giving Retimer Vendors freedom to use the interface of their choice. An example of the interface that can be used is I^2C*.

When this dedicated interface is not used for EEPROM load, and some other means are used to load initial configuration, these pins can be used as Vendor Defined.

3.1.1.3 Miscellaneous Signals

3.1.1.3.1 RX_DET_BYP (PCIe_BYPASS_MODE)

This signal is asserted to bypass the Receiver detection process to expedite the link training. In this mode, the retimer does not do any active determination of its Receiver impedance. It rather assumes that the receiver is present on the other end of the link. This feature can be used for soldered-down devices. The same signal, when asserted, also serves to bypass the PCIe mode.

3.1.1.3.2 REFCLK_Out+/REFCLK_Out-

This is a 100 MHz reference clock as defined by the PCIe Base Specification. Retimer devices are required to provide this clock output to ease clock routing on the platform.

3.1.1.3.3 PERST#

Fundamental Reset signal as defined by the PCIe Base Specification. PERST# assertion puts all Retimer register bits to their default values.

3.1.1.3.4 CLKREQ#

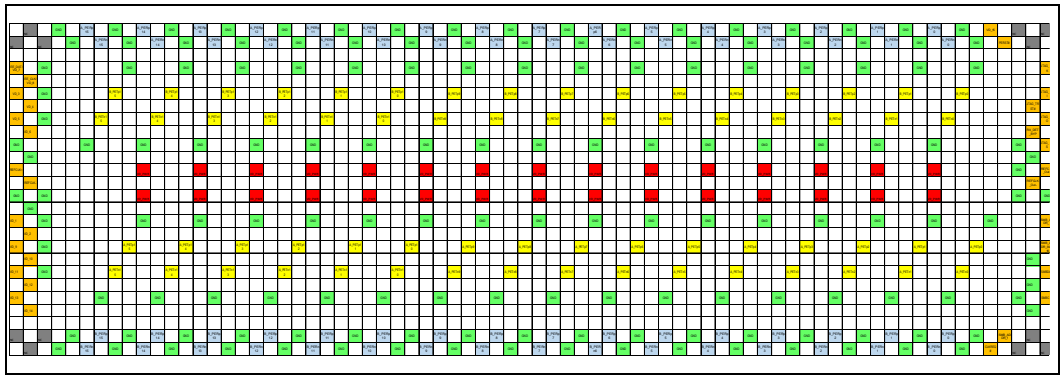
This signal is used to support L1PM Substates. When L1PM substates is not supported by the Platform, this pin must be pulled Low by the retimer in an implementation specific manner. Refer to PCIe Base Specification for more details on L1PM Substate support for retimers.

3.2 x16 Retimer Ballmap (Package Side)

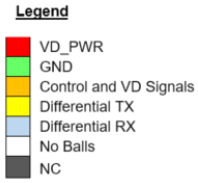
Figure 3-2 shows the ball arrangement from the retimer package side.

Note that this figure is for reference only. For actual pin numbers refer to Figure 3-4, and for spacing details refer to Figure 3-5.

Figure 3-2. x16 Retimer, Package Side Pin Arrangement (Top View)



Note: Refer to Figure 10 for pitch and spacing details.



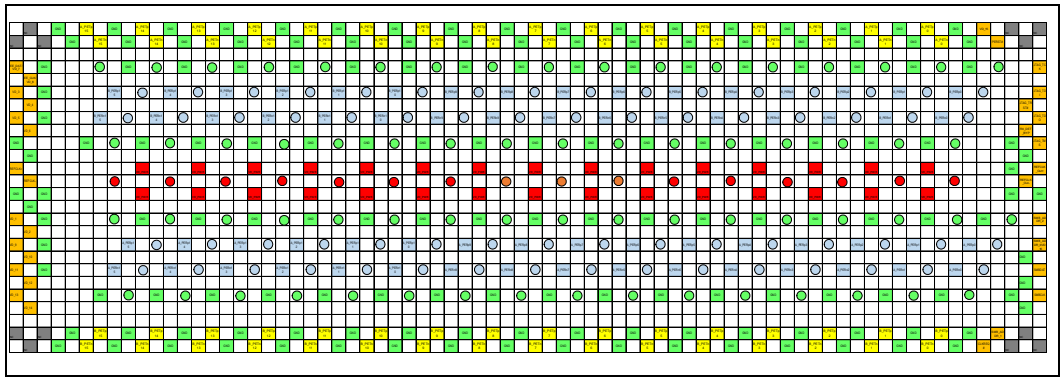
3.3 x16 Retimer Ballmap (Platform Side)

Figure 3-3 shows the platform side pin arrangement with PCB vias. The Transmiter (TX) and Receiver (RX) balls here have been swapped when compared to package side ballmap (Figure 3-2). Meaning that "TX lane x" in the package side ballmap gets mapped to "RX lane x" in the land pattern.

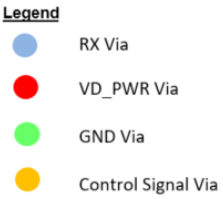
Note that this figure is for reference only. For actual pin numbers refer to Figure 3-4, and for spacing details, refer Figure 3-5.

Implementation Note: It is recommended that the GND PTH vias be located on the platform, as close as possible to the retimer package outer periphery GND pins, to help mitigate the crosstalk.

Figure 3-3. x16 Retimer, Platform side Pin Arrangement (Top View)



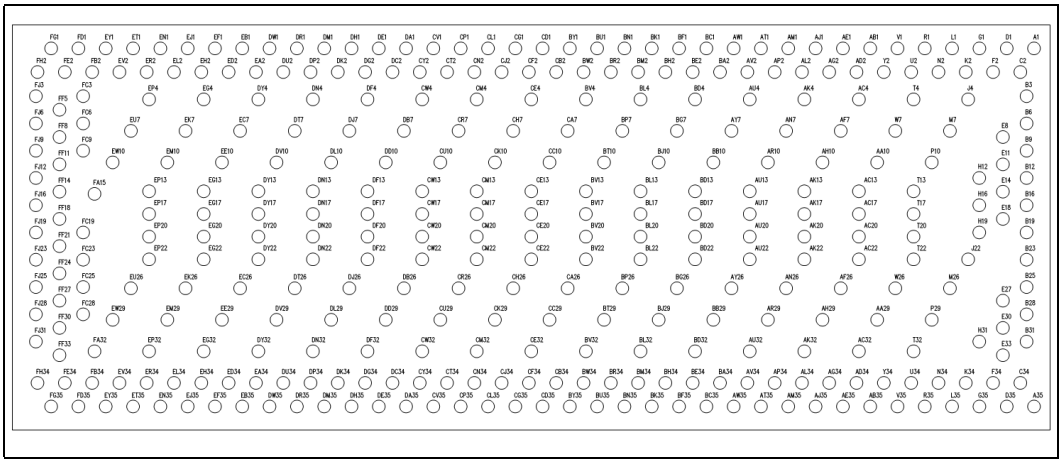
Note: Refer to Figure 3-5 for pitch and spacing details.



3.4 x16 Retimer, Physical Ballmap (Package Side)

Figure 3-4 shows the top view of a x16 Retimer package side ball arrangement with pin numbers. The recommended ball size is 0.3 ±0.05 mm. Refer to Figure 3-5 for spacing requirements between the package side balls. All balls are recommended to be present on the Retimer package. Retimer Vendors may decide to depopulate the corner balls A1 and A35 to avoid package handling issues.

Figure 3-4. x16 Retimer, Physical Ballmap on Package (Top View)

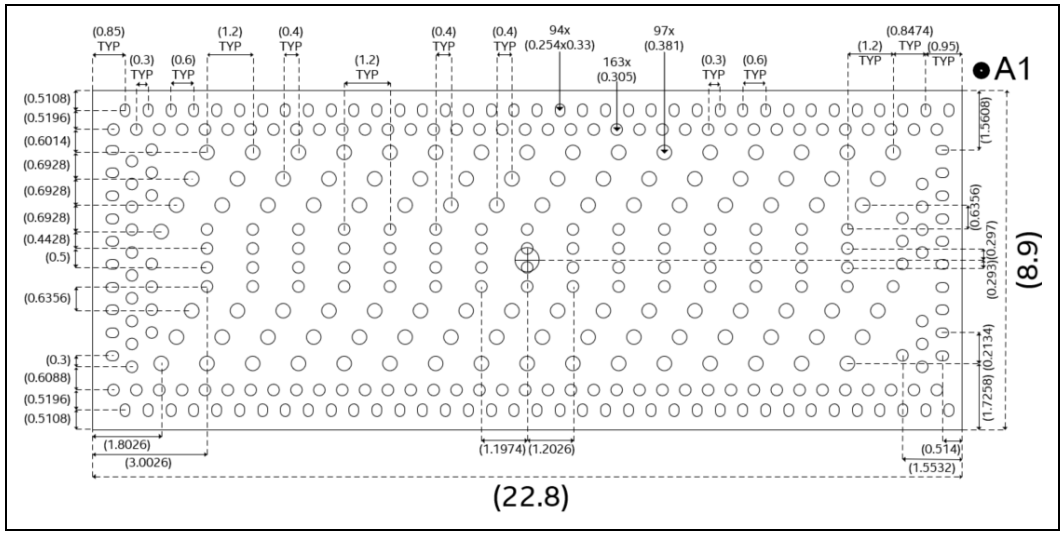


3.5 x16 Retimer Platform Side Land Pattern

Figure 3-5 shows the top view of the platform side mechanical outline drawing for a x16 retimer.

Dimension tolerances for ball diameter are ±0.05 mm.

Figure 3-5. x16 Retimer, platform side land pattern with spacing details (Top View)



Note: All dimensions are in mm, and all distances are center to center.

3.6 x8 Retimer Interface Signals

Table 3-2. x8 Retimer Signal Descriptions

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
High Speed Differential I/Os				
B9	A_PETp0	O	Transmitter differential pair, A Channels, Lane 0	
A10	A_PETn0	O		
C6	A_PETp1	O	Transmitter differential pair, A Channels, Lane 1	
D7	A_PETn1	O		
B3	A_PETp2	O	Transmitter differential pair, A Channels, Lane 2	
A4	A_PETn2	O		
E2	A_PETp3	O	Transmitter differential pair, A Channels, Lane 3	
D1	A_PETn3	O		
AB1	A_PETp4	O	Transmitter differential pair, A Channels, Lane 4	
AA2	A_PETn4	O		
AE4	A_PETp5	O	Transmitter differential pair, A Channels, Lane 5	
AD3	A_PETn5	O		
AH1	A_PETp6	O	Transmitter differential pair, A Channels, Lane 6	
AG2	A_PETn6	O		
AL4	A_PETp7	O	Transmitter differential pair, A Channels, Lane 7	
AK3	A_PETn7	O		
B15	A_PERp0	I	Receiver differential pair, A Channels, Lane 0	
A14	A_PERn0	I		
C18	A_PERp1	I	Receiver differential pair, A Channels, Lane 1	
D17	A_PERn1	I		

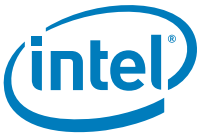


Table 3-2. x8 Retimer Signal Descriptions

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
B21	A_PERp2	I	Receiver differential pair, A Channels, Lane 2	
A20	A_PERn2	I		
E22	A_PERp3	I	Receiver differential pair, A Channels, Lane 3	
D23	A_PERn3	I		
AB23	A_PERp4	I	Receiver differential pair, A Channels, Lane 4	
AA22	A_PERn4	I		
AE20	A_PERp5	I	Receiver differential pair, A Channels, Lane 5	
AD21	A_PERn5	I		
AH23	A_PERp6	I	Receiver differential pair, A Channels, Lane 6	
AG22	A_PERn6	I		
AL20	A_PERp7	I	Receiver differential pair, A Channels, Lane 7	
AK21	A_PERn7	I		
H21	B_PETp0	O	Transmitter differential pair, B Channels, Lane 0	
G20	B_PETn0	O		
L22	B_PETp1	O	Transmitter differential pair, B Channels, Lane 1	
K23	B_PETn1	O		
P21	B_PETp2	O	Transmitter differential pair, B Channels, Lane 2	
N20	B_PETn2	O		
U22	B_PETp3	O	Transmitter differential pair, B Channels, Lane 3	
T23	B_PETn3	O		
AP23	B_PETp4	O	Transmitter differential pair, B Channels, Lane 4	
AN22	B_PETn4	O		
AU20	B_PETp5	O	Transmitter differential pair B Channels, Lane 5	
AT21	B_PETn5	O		
AP17	B_PETp6	O	Transmitter differential pair, B Channels, Lane 6	
AR18	B_PETn6	O		
AU14	B_PETp7	O	Transmitter differential pair, B Channels, Lane 7	
AT15	B_PETn7	O		
H3	B_PERp0	I	Receiver differential pair, B Channels, Lane 0	
G4	B_PERn0	I		
L2	B_PERp1	I	Receiver differential pair, B Channels, Lane 1	
K1	B_PERn1	I		
P3	B_PERp2	I	Receiver differential pair, B Channels, Lane 2	
N4	B_PERn2	I		
U2	B_PERp3	I	Receiver differential pair, B Channels, Lane 3	
T1	B_PERn3	I		
AP1	B_PERp4	I	Receiver differential pair, B Channels, Lane 4	
AN2	B_PERn4	I		
AU4	B_PERp5	I	Receiver differential pair, B Channels, Lane 5	
AT3	B_PERn5	I		

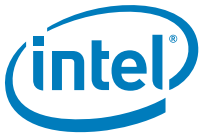


Table 3-2. x8 Retimer Signal Descriptions

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
AP7	B_PERp6	I	Receiver differential pair, B Channels, Lane 6	
AR6	B_PERn6	I		
AU10	B_PERp7	I	Receiver differential pair, B Channels, Lane 7	
AT9	B_PERn7	I		
Reference Clock				
Y5	REFCLK+	I	100MHz. Reference Clock (Differential Pair), as defined by the PCIe Base Specification	
V5	REFCLK-	I		
Y19	REFCLK_Out+ [2]	O	100MHz. This pin is used for driving REFCLK_Out+	
V19	REFCLK_Out- [2]	O	100MHz. This pin is used for driving REFCLK_Out-	
PCI Express Auxiliary Signals				
Y1	PERST#	I	Fundamental Reset; Active Low	1.8 V (3.3 V tolerant)
B11	CLKREQ#	I	Used by L1PM Substates; Active Low	1.8 V (3.3 V tolerant)
JTAG				
AC18	JTAG_TDI	I	JTAG Test Data In	1.8 V
L18	JTAG_TDO	O	JTAG Test Data Out; Open drain; Require pull up to 1.8V on the platform	
E16	JTAG_TMS	I	JTAG Test Mode Select	1.8 V
AG18	JTAG_TCK	I	JTAG Clock	1.8 V
R18	JTAG_TRST#	I	JTAG Reset; Active Low	1.8 V
System Management Bus (SMBus)				
AC6	SMBCLK	I/O	SMBus Clock Input / Open Drain Clock Output	1.8 V (3.3 V tolerant)
AG6	SMBDAT	I/O	SMBus Data Input / Open Drain Output	1.8 V (3.3 V tolerant)
R6	SMB_ADDR_1	I	SMBus Address Bit 1	1.8 V (3.3 V tolerant)
L6	SMB_ADDR_2	I	SMBus Address Bit 2	1.8 V (3.3 V tolerant)
V23	SMB_ADDR_3 / VD_12	I	SMBus Address Bit3 or Vendor Defined	1.8 V (3.3 V tolerant)
EEPROM Configuration Interface				
AP11	EE_CLK/ VD_5 [1]	I/O	EEPROM Interface clock or Vendor Defined	1.8 V (3.3 V tolerant)
AP13	EE_DAT/ VD_6 [1]	I/O	EEPROM Interface data or Vendor Defined	1.8 V (3.3 V tolerant)
Miscellaneous				
AT1	VD_1	TBD	Vendor Defined Signal	
W2	VD_2	TBD	Vendor Defined Signal	
B1	VD_3	TBD	Vendor Defined Signal	
AU12	VD_4	TBD	Vendor Defined Signal	
D11	VD_7 [1]	TBD	Vendor Defined Signal	
D13	VD_8 [1]	TBD	Vendor Defined Signal	

Table 3-2. x8 Retimer Signal Descriptions

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
A12	VD_9	TBD	Vendor Defined Signal	
W22	VD_10	TBD	Vendor Defined Signal	
AT23	VD_11	TBD	Vendor Defined Signal	
B23	VD_13	TBD	Vendor Defined Signal	
AT13	RX_DET_BYP	I	Receiver Detection Bypass	1.8 V(3.3 V tolerant)
Power				
64 pins	VD_PWR[3]		Vendor Defined Power: These ball are assigned for Power only. The actual voltage on specific balls and the tolerance is to be decided between the Platform Vendor and the Retimer Vendor.	
175 pins	GND[3]		0 V	

Notes:
1. It is safe to route high speed Vendor Defined signals at these locations. Rest VD pins are recommended to be used for static signals. Routing high frequency/low frequency signals on these may impose crosstalk on high-speed signals. Retimer vendors are recommended to do a thorough signal integrity analysis when using any of the VD pins. Detailed SI analysis should be performed to decide whether unused VD pins can be left floating or need to be terminated or grounded on the platform side/Retimer side.
2. REFCLK Out is compliant with REFCLK definition in the PCIe Base Specification.
3. Refer to Section 7.2, "Pin List for x8 (Package Side) Pinout" for complete list of x8 pins.

3.6.1 Signal Descriptions

3.6.1.1 SMBus Interface

Refer to Section 3.1.1.1, "SMBus Interface".

3.6.1.2 EEPROM Interface

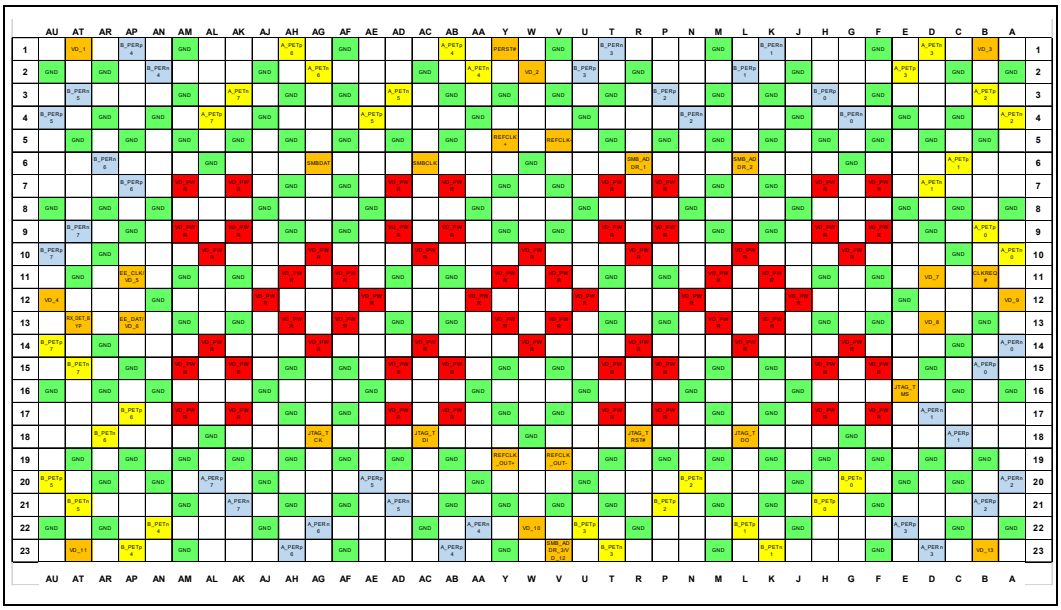
Refer to Section 3.1.1.2, "EEPROM Interface".

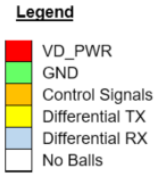
3.6.1.3 Miscellaneous Signals

Refer to Section 3.1.1.3, "Miscellaneous Signals".

3.7 x8 Retimer Ballmap (Package Side)

Figure 3-6. x8 Retimer, Package Side Pin Arrangement (Top View)



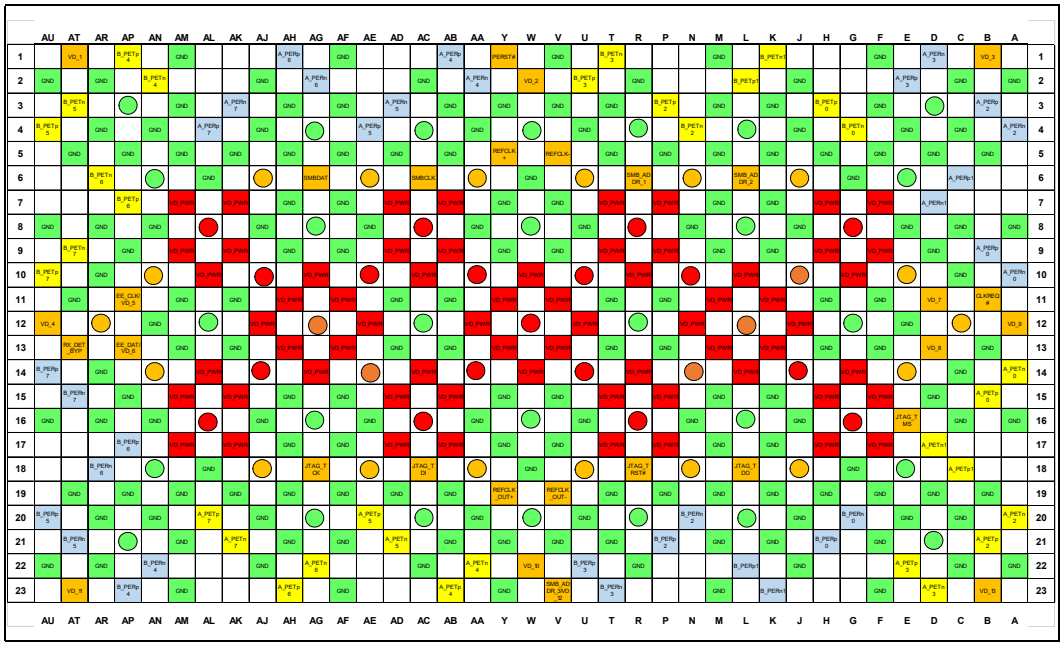


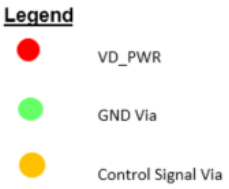
3.8 x8 Retimer Ballmap (Platform Side)

Figure 3-7 shows the platform side land pattern. The TX and RX balls have been swapped when compared to the package side ballmap. Meaning that the “TX lane x” in the package side ballmap gets mapped to “RX lane x” in the land pattern.

Implementation Note: It is recommended that the GND PTH vias be located on the platform, as close possible to the Retimer package outer periphery GND pins, to help mitigate the crosstalk.

Figure 3-7. x8 Retimer, Platform side Pin Arrangement (Top View)

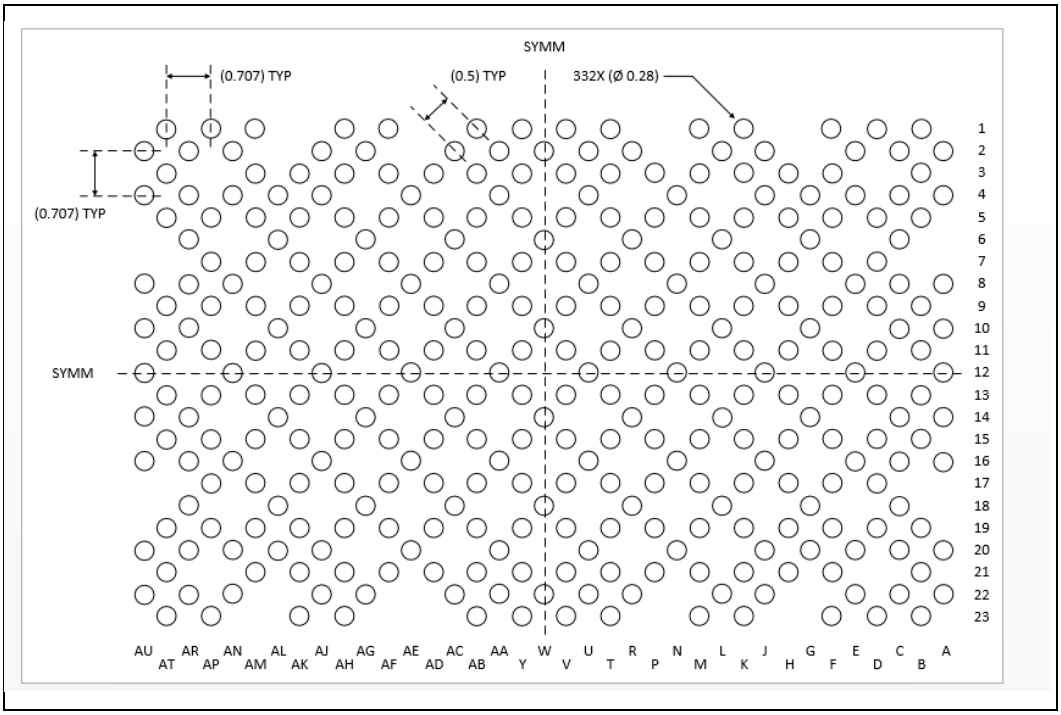




3.9 x8 Retimer, Physical Ballmap (Package Side)

Figure 3-8 shows the top view of a x8 Retimer package side ball arrangement with ball spacing. The recommended ball size is 0.28 ±0.05 mm.

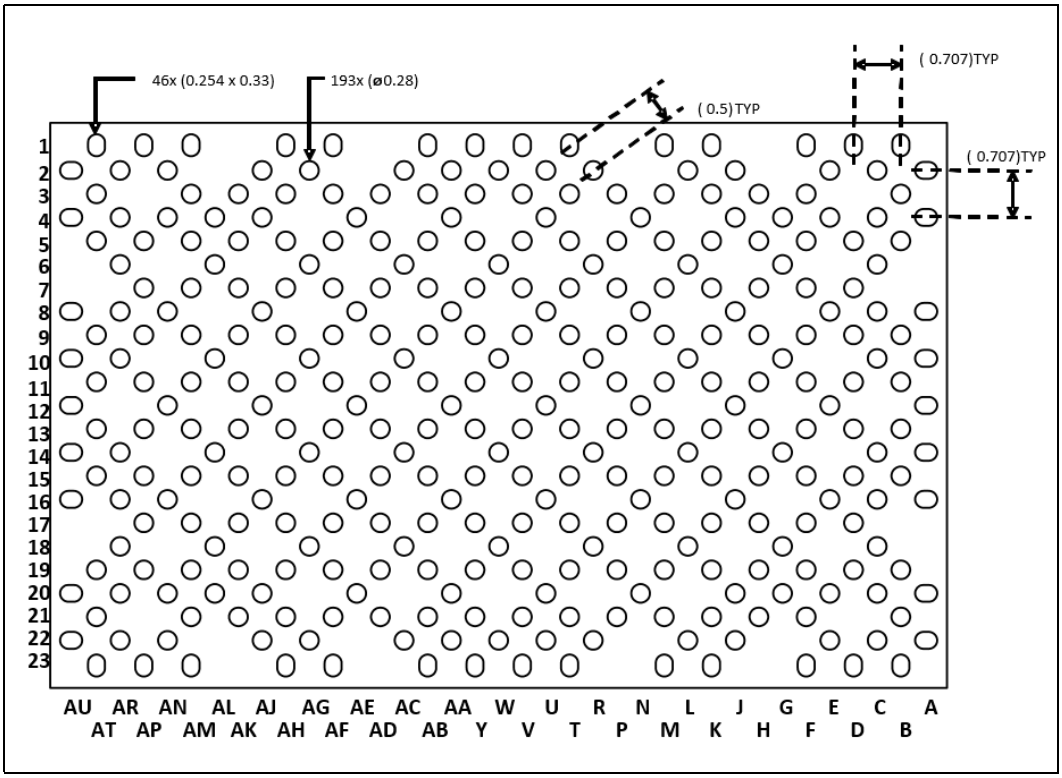
Figure 3-8. x8 Retimer, Physical Ballmap on Package (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.10 x8 Retimer Platform Side Land Pattern

Figure 3-9. x8 Retimer, Platform side Land Pattern with spacing details (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.11 x4 Retimer Interface Signals

Table 3-3. x4 Retimer Signal Descriptions (Sheet 1 of 3)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
High Speed Differential I/Os				
A3	A_PETp0	O	Transmitter differential pair, A Channels, Lane 0	
A4	A_PETn0	O		
C1	A_PETp1	O	Transmitter differential pair, A Channels, Lane 1	
B1	A_PETn1	O		
F1	A_PETp2	O	Transmitter differential pair, A Channels, Lane 2	
E1	A_PETn2	O		
J1	A_PETp3	O	Transmitter differential pair, A Channels, Lane 3	
H1	A_PETn3	O		
A8	A_PERp0	I	Receiver differential pair, A Channels, Lane 0	
A7	A_PERn0	I		

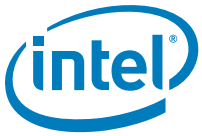


Table 3-3. x4 Retimer Signal Descriptions (Sheet 2 of 3)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
C10	A_PERp1	I	Receiver differential pair, A Channels, Lane 1	
B10	A_PERn1	I		
F10	A_PERp2	I	Receiver differential pair, A Channels, Lane 2	
E10	A_PERn2	I		
J10	A_PERp3	I	Receiver differential pair, A Channels, Lane 3	
H10	A_PERn3	I		
M10	B_PETp0	O	Transmitter differential pair, B Channels, Lane 0	
L10	B_PETn0	O		
R10	B_PETp1	O	Transmitter differential pair, B Channels, Lane 1	
P10	B_PETn1	O		
V10	B_PETp2	O	Transmitter differential pair, B Channels, Lane 2	
U10	B_PETn2	O		
W7	B_PETp3	O	Transmitter differential pair, B Channels, Lane 3	
W8	B_PETn3	O		
M1	B_PERp0	I	Receiver differential pair, B Channels, Lane 0	
L1	B_PERn0	I		
R1	B_PERp1	I	Receiver differential pair, B Channels, Lane 1	
P1	B_PERn1	I		
V1	B_PERp2	I	Receiver differential pair, B Channels, Lane 2	
U1	B_PERn2	I		
W4	B_PERp3	I	Receiver differential pair, B Channels, Lane 3	
W3	B_PERn3	I		
Reference Clock				
C5	REFCLK+	I	100 MHz. Reference Clock (Differential Pair), as defined by the PCIe Base Specification	
C6	REFCLK-	I		
U5	REFCLK_Out+ [2]	O	100 MHz. This pin is used for driving REFCLK_out+	
U6	REFCLK_Out- [2]	O	100 MHz. This pin is used for driving REFCLK_Out-	
PCI Express Auxiliary Signals				
A2	PERST#	I	Fundamental Reset; Active Low	1.8 V (3.3 V tolerant)
A9	CLKREQ#	I	Used by L1PM Substates; Active Low	1.8 V (3.3 V tolerant)
JTAG				
U3	JTAG_TDI	I	JTAG Test Data In	1.8 V
C3	JTAG_TDO	O	JTAG Test Data Out; Open drain; Requires pull up 1.8V on the platform	
N3	JTAG_TMS	I	JTAG Test Mode Select	1.8 V
K3	JTAG_TCK	I	JTAG Clock	1.8 V (
G3	JTAG_TRST#	I	JTAG Reset; Active Low	1.8 V (
System Management Bus (SMBus)				
G8	SMBCLK	I/O	SMBus Clock Input / Open Drain Clock Output	1.8 V (3.3 V tolerant)

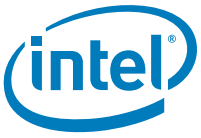


Table 3-3. x4 Retimer Signal Descriptions (Sheet 3 of 3)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
K8	SMBDAT	I/O	SMBus Data Input / Open Drain Output	1.8 V (3.3 V tolerant)
W5	SMB_ADDR_1	I	SMBus Address Bit 1	1.8 V (3.3 V tolerant)
W6	SMB_ADDR_2	I	SMBus Address Bit 2	1.8 V (3.3 V tolerant)
W9	SMB_ADDR_3 /VD_10	I	SMBus Address Bit 3 or Vendor Defined	1.8 V (3.3 V tolerant)
EEPROM Configuration Interface				
U8	EE_DAT/ VD_7[1]	I/O	EEPROM Interface data or Vendor Defined	1.8 V(3.3 V tolerant)
N8	EE_CLK/ VD_8[1]	I/O	EEPROM Interface clock or Vendor Defined	1.8 V(3.3 V tolerant)
Miscellaneous				
W1	VD_1	TBD	Vendor Defined Signal	
W2	VD_2	TBD	Vendor Defined Signal	
W10	VD_3	TBD	Vendor Defined Signal	
A1	VD_4	TBD	Vendor Defined Signal	
A5	VD_5	TBD	Vendor Defined Signal	
A10	VD_6	TBD	Vendor Defined Signal	
C8	VD_9	TBD	Vendor Defined Signal	
A6	RX_DET_BYP	I	Receiver Detection Bypass	1.8 V(3.3 V tolerant)
Power				
34 pins	VD_PWR[3]		Vendor Defined Power: These balsl are assigned for Power only. The actual voltage on specific balls and the tolerance is to be decided between the Platform Vendor and the Retimer Vendor.	
54 pins	GND[3]		0 V	

Notes:
1. It is safe to route high speed Vendor Defined signals at these locations. Rest VD pins are recommended to be used for static signals. Routing high frequency/low frequency signals on these may impose crosstalk on high-speed signals. Retimer Vendors are recommended to do a thorough signal integrity analysis when using any of the VD pins. Detailed SI analysis should be performed to decide whether unused VD pins can be left floating or need to be terminated or grounded on the platform side/Retimer side.
2. REFCLK Out is compliant with REFCLK definition in the PCIe Base Specification.
3. Refer to Section 7.3, "Pin List for x4 (Package Side) Pinout" for complete list of x4 pins.

3.11.1 Signal Descriptions

3.11.1.1 SMBus Interface

Refer to Section 3.1.1.1, "SMBus Interface".

3.11.1.2 EEPROM Interface

Refer to Section 3.1.1.2, "EEPROM Interface".

3.11.1.3 Miscellaneous Signals

Refer to Section 3.1.1.3, "Miscellaneous Signals".

3.12 x4 Retimer Ballmap (Package Side)

Figure 3-10. x4 Retimer, Package Side Pin Arrangement (Top View)

	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	VD_1	B_PERp 2	B_PERn 2	GND	B_PERp1	B_PERn1	GND	B_PERp 0	B_PERn 0	GND	A_PETp 3	A_PETn 3	GND	A_PETp 2	A_PETn 2	GND	A_PETp1	A_PETn1	VD_4	1
2	VD_2		GND		GND	GND		GND	GND		GND	GND		GND	GND		GND		PERST#	2
3	B_PERn 3	GND	JTAG_T DI	VD_PWR	VD_PWR	VD_PWR	JTAG_T MS	VD_PWR	VD_PWR	JTAG_T CK	VD_PWR	VD_PWR	JTAG_T RST#	VD_PWR	VD_PWR	VD_PWR	JTAG_T DO	GND	A_PETp 0	3
4	B_PERp 3	GND		VD_PWR		VD_PWR		VD_PWR		VD_PWR		VD_PWR		VD_PWR		VD_PWR		GND	A_PETn 0	4
5	SMB_AD DR_1	GND	REFCLK _OUT+		GND		GND		GND		GND		GND		GND		REFCLK +	GND	VD_5	5
6	SMB_AD DR_2	GND	REFCLK _OUT-		GND		GND		GND		GND		GND		GND		REFCLK-	GND	RX_DET _BYP	6
7	B_PETp 3	GND		VD_PWR		VD_PWR		VD_PWR		VD_PWR		VD_PWR		VD_PWR		VD_PWR		GND	A_PERn 0	7
8	B_PETn 3	GND	EE_DAT/ VD_7	VD_PWR	VD_PWR	VD_PWR	EE_CLK/ VD_8	VD_PWR	VD_PWR	SMBDAT	VD_PWR	VD_PWR	SMBCLK	VD_PWR	VD_PWR	VD_PWR	VD_9	GND	A_PERp 0	8
9	SMB_AD DR_3/VD _10		GND		GND	GND		GND	GND		GND	GND		GND	GND		GND		CLKREQ #	9
10	VD_3	B_PETp 2	B_PETn 2	GND	B_PETp1	B_PETn1	GND	B_PETp 0	B_PETn 0	GND	A_PERp 3	A_PERn 3	GND	A_PERp 2	A_PERn 2	GND	A_PERp1	A_PERn1	VD_6	10
	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Legend

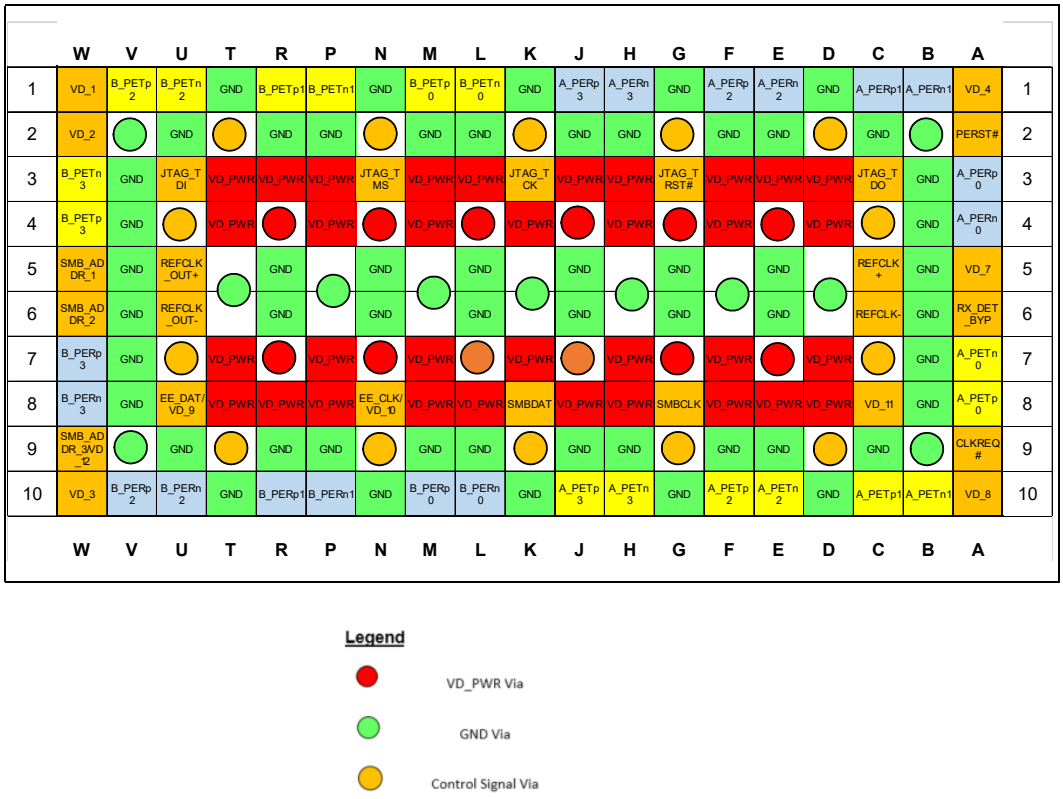
- VD_PWR
- GND
- Control Signals
- Differential TX
- Differential RX
- No Balls

3.13 x4 Retimer Ballmap (Platform side)

Figure 3-11 shows the platform's side land pattern. The TX and RX balls have been swapped when compared to the package side ballmap. Meaning that the "X lane x" in the package side ballmap gets mapped to "RX lane x" in the land pattern.

Implementation Note: It is recommended that the GND PTH vias be located on the platform, as close possible to the retimer package outer periphery GND pins, to help mitigate the crosstalk.

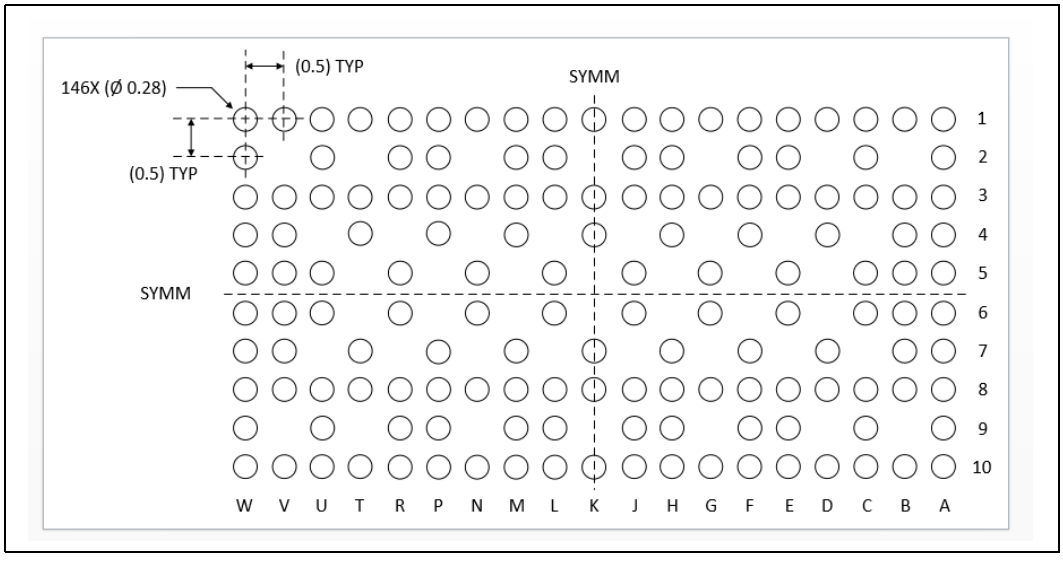
Figure 3-11. x4 Retimer, Platform side Land Pattern (Top View)



3.14 x4 Retimer, Physical Ballmap (Package side)

Figure 3-12 shows the top view a of x4 Retimer package side ball arrangement with ball spacing. The recommended ball size is 0.28 ±0.05 mm.

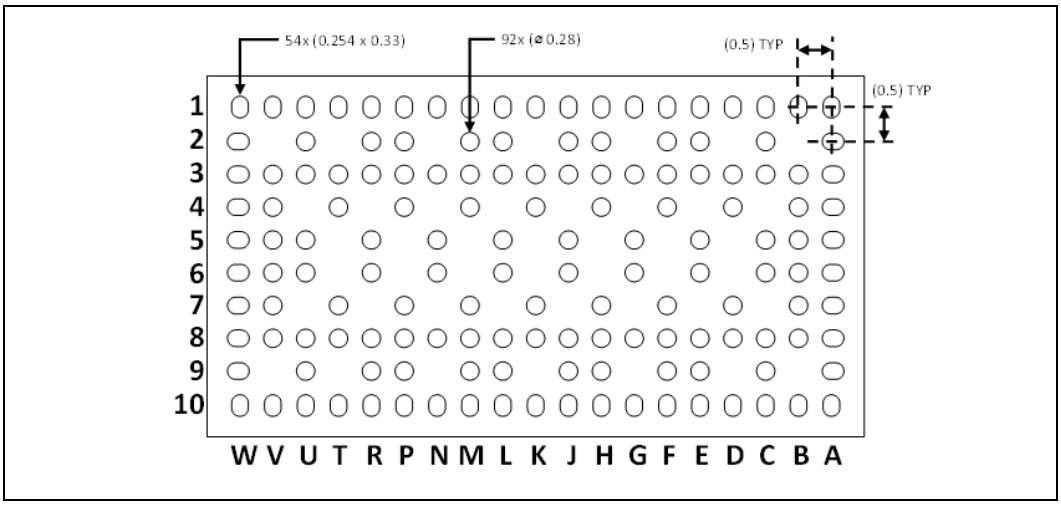
Figure 3-12. x4 Retimer, Physical Ballmap on Package (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.15 x4 Retimer Platform side Land Pattern

Figure 3-13. x4 Retimer, Platform side Land Pattern with spacing details (Top View)



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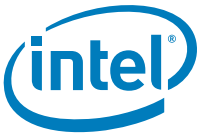


4 Electrical Characteristics

No particular power supply rails are specified due to different process nodes used by various Retimer vendors. There are balls in the Retimer ball map that are reserved for VD_PWR (Vendor defined power). These are the only balls that must be used to supply power to the Retimer.

Actual voltage, tolerances and power sequencing for various power rails used is to be decided between the Retimer Vendor and the System Vendor.

It is recommended that the Transmitter AC coupling capacitors (Refer to the PCIe Base Specification) be located inside the Retimer package for both the upstream and downstream pseudo port Transmitters.

The Platform designer will have to consider the options and ensure the requirements are met for the specific Retimer they are working with.

4.1 Power Consumption

Table 4-1 lists the power consumption values under maximum operating conditions. Maximum power is consumed when all the lanes are operating at 32 GT/s with full swing on Transmitter. Refer to Section 4.4 for details on Thermal requirements.

Table 4-1. Recommended Absolute Maximum Power Ratings

	Max. Total Power Consumption for all Power rails	Unit
x16	16	W
x8	8	W
x4	4	W

4.2 Power Supply Decoupling

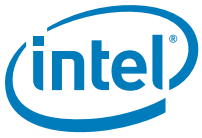
Due to the low level signaling of the PCIe interface, it is strongly recommended that sufficient decoupling of all power supplies be provided. It is recommended to ensure that power supply noise does not interfere with the recovery of data from a remote upstream PCIe device.

It is the responsibility of the Retimer designer and the Platform designer to properly design and test the power supply decoupling to ensure that Retimer circuitry does not create excessive noise on the power supply or ground signals at the Retimer package balls.

It is recommended that the Retimer Vendor incorporates the decoupling caps in the package or in the die, as they are needed to minimize noise at the package balls.

4.3 Retimer Latency

Maximum Latency (Refer to the PCIe Base Specification) for PCIe 5.0 retimers is from 48.5 to 61.5 ns, depending on clocking architecture and maximum payload size. Some applications may need significantly lower latency (less than 10 ns). OEMs are recommended to work with Retimer Vendors for this low latency use case.



4.4 Package Thermal considerations

Junction temperature TJ(max) will be different for different market segments or use conditions. For example, 100-105 °C, 100-110 °C, 110-125 °C.

The allowed temperature TJ(max) is application-dependent and needs to be considered by the Retimer Designers. These details are outside the scope of this specification.

Ambient temperature TA indicates the local ambient temperature operating range.

Commercial temperature range (Climate controlled) is from 0°C to 70°C, whereas extended temperature range (non-Climate controlled) is from -40 °C to 85 °C. Whether commercial or extended temperature range is applicable is dependent upon the application/use condition.

Detailed thermal analysis including heatsink requirements are outside the scope of this specification. The Retimers will be used in a variety of chassis types/Platforms. It is up to the Retimer Vendor and the OEM to figure out thermal/heatsink requirements based on the chassis type and specific location on the chassis for the retimer.

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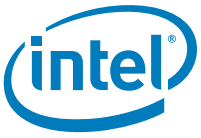

5 BSMBus and EEPROM

It is recommended that each Retimer has a dedicated EEPROM behind it, from where the retimer loads its configuration data upon power up. A dedicated EEPROM interface allows the Retimer to use a fixed address to access the EEPROM.

It is recommended that the Retimer loads the configuration through EEPROM. Once the EEPROM configuration is loaded, if any additional configuration changes are needed, it is done using the SMBus interface from the platform side.

If the Retimer is located on a CEM riser card, it is not possible for the Platform to program the retimer using SMBus interface, as the platform does not know the Retimer address. In that case, the Retimer (located on CEM riser card) is required to have a dedicated EEPROM associated with it. It should be noted that, once the retimer loads the configuration from this EEPROM, it cannot be changed using SMBus commands from the platform.

The Retimer pinout supports 3 SMBus address pins, allowing up to 8 addressable devices on the bus. If more than 8 devices (and hence addresses) are needed, some kind of SMBus multiplexing is to be used on the platform side. Details of how SMBus multiplexing and addressing is done on the platform is left to be implementation specific.

It is recommended to minimize the configurations through SMBus in applications where boot time is to be minimized.

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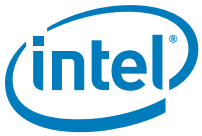


6 Register Configuration

6.1 SMBus Address Range

Retimer SMBus addresses will be chosen from the range 20h to 27h.

Table 6-1 shows the bit level mapping for the SMBus address byte.

Table 6-1. SMBus Address bits Mapping

Address bit	Address Bit Value
1	SMB_ADDR_1
2	SMB_ADDR_2
3	SMB_ADDR_3
4	0
5	0
6	1
7	0

6.2 SMBus Command Formats

The SMBus Interface responds to following SMBus commands.

Refer to the SMBus specification for a detailed description of these commands.

- Block Write/Read with PEC.

Table 6-2 defines the command code associated with retimer SMBus transactions.

Table 6-2. Slave SMBus Command Code Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PEC	RSVD		FUNCTION			START	END

Table 6-3. Slave SMBus Command Code Fields

Bit Field	Name	Description
0	END	End of transaction indicator. Setting both START and END signifies a single transaction sequence. 0 - Current transaction is not the last read or write sequence. 1 - Current transaction is the last read or write sequence. Refer to Table 6-4 for usage of this bit.
1	START	Start of transaction indicator. Setting both START and END signifies a single transaction sequence 0 - Current transaction is not the first of a read or write sequence. 1 - Current transaction is the first of a read or write sequence. Refer to Table 6-4 for usage of this bit.

Table 6-3. Slave SMBus Command Code Fields

Bit Field	Name	Description
4:2	FUNCTION	This field encodes the type of SMBus operation. 000 - Retimer register read operation 001 - Retimer register write operation 010 - Vendor defined 011 - Vendor defined 100 - Vendor defined 101 - Vendor defined 110 - Vendor defined 111 - Vendor defined
6:5	RSVD	This field is Reserved
7	PEC	This bit controls whether packet error checking is enabled for the current SMBus transaction. 0 - Packet error checking disabled for the current SMBus transaction. 1 - Packet error checking enabled for the current SMBus transaction.

START (Bit Field 1) and END (Bit Field 0) are used to indicate if the SMBus command spans across multiple transactions.

Table 6-4. START and END bit usage for command code

START bit value	END bit value	Description
1	0	This is the first transaction in a command that spans across multiple transactions
0	1	This is the last transaction in a command that spans across multiple transactions
1	1	SMBus command is implemented using a single transaction
0	0	Reserved

6.3 SMBus Block Read/Write Examples

All read and write accesses to the registers should be 32 bits, as shown in the following examples.

Non-shaded items in the examples are driven by SMBus Host, and the shaded items are driven by SMBus Slave implementation on the retimer.

6.3.1 Read Vendor ID (Implemented using Block Read with repeat START)

S	Retimer Slave SMBus Address	Wr	A	CCODE START, READ, PEC (82)	A	BYTC NT=2	A	Offset Lower Byte (04)	A	Offset Upper Byte (00)	A	PEC	A	P

S	Retimer Slave SMBus Address	Wr	A	CCODE END, READ, PEC (81)	A	Sr	Retimer Slave SMBus Address	Rd	A	BYTCNT=6	A

Offset Lower Byte (04)	A	Offset Upper Byte (00)	A	DATA Lower Byte (7:0)	A	DATA Lower Byte (15:8)	A	DATA Upper Byte (23:16)	A	DATA Upper Byte (31:24)	A	PEC	N	P

6.3.2 Write 16G Preset (P7) for Downstream Pseudo Port

S	Retimer Slave SMBus Address	Wr	A	CCODE START, END, WRITE, PEC (87)	A	BYT CNT=6	A	Offset Lower Byte (14)	A	Offset Upper Byte (00)	A	DATA Lower Byte (7:0)	A	DATA Lower Byte (15:8)	A	DATA Upper Byte (23:16)

A	DATA Upper Byte (31:24)	A	PEC	A	P

6.3.3 Enable SRIS (Implemented using Block Write)

S	Retimer Slave SMBus Address	Wr	A	CCODE START, END, WRITE, PEC (87)	A	BYTCNT=6	A

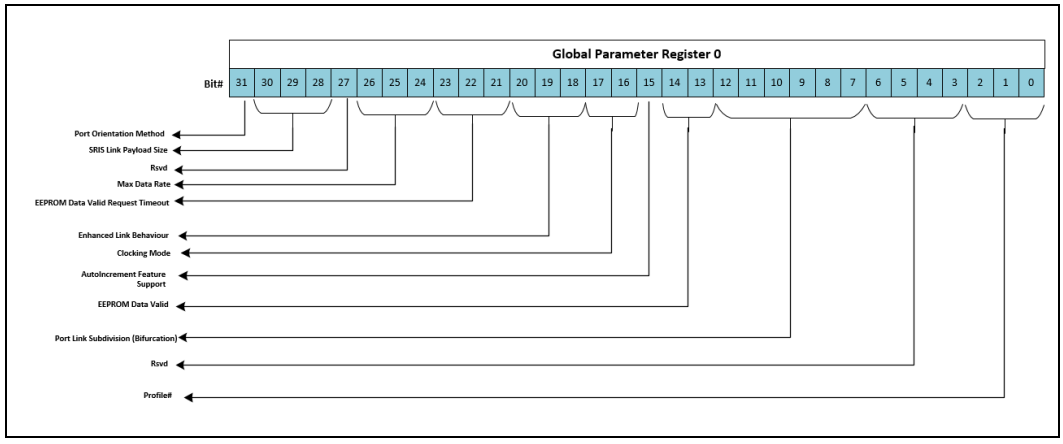
Offset Lower Byte (10)	A	Offset Upper Byte (00)	A	DATA Lower Byte (7:0)	A	DATA Lower Byte (15:8)	A	DATA Upper Byte (23:16)	A	DATA Upper Byte (31:24)	A	PEC	A	P

If the retimer sends NACK for any of the commands because it is not ready to write or read the data from specified offset location, the entire command needs to be repeated.

If the retimer supports the optional auto-increment feature, it can indicate the support by using a bit in the Global Parameter Register 0.

6.4 Global Parameter Register 0

Figure 6-1. Global Parameter Register 0



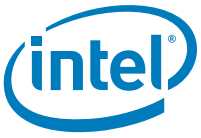


Table 6-5. Global Parameter Register 0

Bit Location	Register Description	Attributes	Description
2:0	**Profile#** 000: Rev 4.0 Ver 0.5 001: Rev 4.0 Ver 0.7+ 010: Rev 5.0 Ver 0.5 011: Rev 5.0 Ver 0.7 100-111: Reserved for future versions	RO	This field indicates which Retimer common footprint specification revision and version the retimer is implementing. Register configuration might be different across different revisions and versions.
6:3	Rsvd	RO	Reserved for future use
12:7	**Port Link Subdivision (Bifurcation)** 000000: _ _ _ x16 (15:0 as x16) (Def) 000001: _ _ x8 (7:0 as x8) 000010: _ _ _ x4 (3:0 as x4) 000011: _ x8 _ x8 (15:8 as x8, 7:0 as x8) 000100: _ x8 x4 x4 (15:8 as x8, 7:4 as x4, 3:0 as x4) 000101: x4 x4 _ x8 (15:12 as x4, 11:8 as x4, 7:0 as x8) 000110: x4 x4 x4 x4 (15:12 as x4, 11:8 as x4, 7:4 as x4, 3:0 as x4) 000111: x2 x2 x2 x2 x2 x2 x2 x2 (15:14 as x2, 13:12 as x2, 11:10 as x2, 9:8 as x2, 7:6 as x2, 5:4 as x2, 3:2 as x2, 1:0 as x2) 001000: x8 x4 x2 x2 (15:8 as x8, 7:4 as x4, 3:2 as x2, 1:0 as x2) 001001: x8 x2 x2 x4 (15:8 as x8, 7:6 as x2, 5:4 as x2, 3:0 as x4) 001010:x2 x2x4 x8 (15:14 as x2, 13:12 as x2, 11:8 as x4, 7:0 as x8) 001011: x4 x2 x2 x8 (15:12 as x4, 11:10 as x2, 9:8 as x2, 7:0 as x8) 001100: x2 x2 x2 x2 x8 (15:14 as x2, 13:12 as x2, 11:10 as x2, 9:8 as x2, 7:0 as x8) 001101: x8 x2 x2 x2 x2 (15:8 as x8, 7:6 as x2, 5:4 as x2, 3:2 as x2, 1:0 as x2) 001110: x2 x2 x4 x4 x4 (15:14 as x2, 13:12 as x2, 11:8 as x4, 7:4 as x4, 3:0 as x4) 001111: x4 x2 x2 x4 x4 (15:12 as x4, 11:10 as x2, 9:8 as x2, 7:4 as x4, 3:0 as x4) 010000: x4 x4 x2 x2 x4 ((15:12 as x4, 11:8 as x4, 7:6 as x2, 5:4 as x2, 3:0 as x4) 010001: x4 x4 x4 x2 x2 (15:12 as x4, 11:8 as x4, 7:4 as x4, 3:2 as x2, 1:0 as x2)	RWS	These bits indicate which link division scheme the end points connected to the retimer support. The host reads this register and updates it's port link subdivision to reflect this. How retimer determines the link sub-division requirements for end-points is outside the scope of this specification. Once the settings are updated in this register, issuing a Global Soft Reset applies the updated link subdivision.

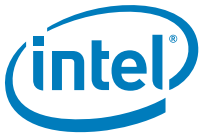


Table 6-5. Global Parameter Register 0 (Continued)

Bit Location	Register Description	Attributes	Description
	010010: x2 x2 x2 x2 x4 x4 (15:14 as x2, 13:12 as x2, 11:10 as x2, 9:8 as x2, 7:6 as x2, 5:4 as x2, 3:0 as x4) 010011: x2 x2 x4 x2 x2 x4 (15:14 as x2, 13:12 as x2, 11:8 as x4, 7:6 as x2, 5:4 as x2, 3:0 as x4) 010100: x4 x2 x2 x2 x2 x4 (15:12 as x4, 11:10 as x2, 9:8 as x2, 7:6 as x2, 5:4 as x2, 3:0 as x4) 010101: x2 x2 x4 x4 x2 x2 (15:14 as x2, 13:12 as x2, 11:8 as x4, 7:4 as x4, 3:2 as x2, 1:0 as x2) 010110: x4 x2 x2 x4 x2 x2 (15:12 as x4, 11:10 as x2, 9:8 as x2, 7:4 as x4, 3:2 as x2, 1:0 as x2) 010111: x4 x4 x2 x2 x2 x2 (15:12 as x4, 11:8 as x4, 7:6 as x2, 5:4 as x2, 3:2 as x2, 1:0 as x2) 011000: x2 x2 x2 x2 x2 x2 x4 (15:14 as x2, 13:12 as x2, 11:10 as x2, 9:8 as x2, 7:6 as x2, 5:4 as x2, 3:0 as x4) 011001: x2 x2 x2 x2 x4 x2 x2 (15:14 as x2, 13:12 as x2, 11:10 as x2, 9:8 as x2, 7:4 as x4, 3:2 as x2, 1:0 as x2) 011010: x2 x2 x4 x2 x2 x2 x2 (15:14 as x2, 13:12 as x2, 11:8 as x4, 7:6 as x2, 5:4 as x2, 3:2 as x2, 1:0 as x2) 011011: x4 x2 x2 x2 x2 x2 x2 (15:12 as x4, 11:10 as x2, 9:8 as x2, 7:6 as x2, 5:4 as x2, 3:2 as x2, 1:0 as x2) 011100: x4 x4 (7:4 as x4, 3:0 as x4) 011101: x2 x2 x4 (7:6 as x2, 5:4 as x2, 3:0 as x4) 011110: x4 x2 x2 (7:4 as x4, 3:2 as x2, 1:0 as x2) 011111: x2 x2 x2 x2 (7:6 as x2, 5:4 as x2, 3:2 as x2, 1:0 as x2) 100000: x2 x2 (3:2 as x2, 1:0 as x2)		
14:13	**EEPROM Data Valid** 00: No EEPROM (Def) 01: EEPROM Present and Data Valid 10: EEPROM Present and Data Not Valid 11: Controller Busy*	RO	This bit indicates if the external EEPROM data is valid or not.
15	**AutoIncrement Feature Support** 1: Supported 0:Not Supported (Def)	RO	Auto increment feature supports splitting the read or write transactions into multiple byte read or write transactions, START and STOP bits as defined in Table 6.3 are used when Auto-increment feature is supported.
17:16	**Clocking Mode** 00 : Common Clock (Def) 01 : SRIS 10 : SRNS 11 : Reserved	RWS	These bits indicate whether the Retimer supports Common Clock or Separate clock architecture. Any updates to this register are applicable after Global Soft Reset.

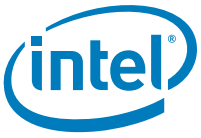


Table 6-5. Global Parameter Register 0 (Continued)

Bit Location	Register Description	Attributes	Description
20:18	**Enhanced Link Behavior** Bit 20: 'Modified TS1/TS2 Ordered Sets' supported. Bit 19: 'No Equalization Needed' mode supported. A device advertising this capability must support 'Equalization Bypass to Highest Rate.' Bit 18: 'EQ Bypass to Highest Rate' mode supported. 3'b010, 3'b110 are not allowed.	RWS	This controls the ability for the Retimer to either bypass equalization to the highest data rate or completely bypass equalization when it supports 32.0 GT/s. Any updates to this register are applicable after Global Soft Reset.
23:21	**EEPROM Data valid Request Timeout** 000: no delay 001: 10ms (Def) 010: 20ms 011: 30ms 100: 40ms 101: 50ms 110: 60ms 111:70ms	RO	If the Controller is busy (EEPROM Valid bit = 11), then the next read operation can be tried after time set in this Timeout field.
26:24	**Max Data Rate** 000: Rsvd 001: 2.5 G (Def) 010: 5.0 G 011: 8.0 G 100: 16 G 101: 32 G 110: Rsvd 111: Rsvd	RW	These bits control the maximum data rate that the Retimer sets in the Data Rate Identifier field of training sets that the Retimer transmits.
27	Rsvd	RO	Reserved for future use
30:28	**SRIS Link Payload Size** (valid when Bit3=1) 000: 128 001: 256 010: 512 011: 1024 100: 2048 101: 4096 (Def) 110: Rsvd 111: Rsvd	RWS	This controls the maximum payload size the Retimer supports while in SRIS. Retimers that do not support SRIS are not required to provide this configuration parameter. Any updates to this register are applicable after Global Soft Reset.
31	**Port Orientation Method** 0: Static 1: Dynamic (Def)	RWS	Determines whether the Port Orientation is determined dynamically or statically. Check out PCie Base specification for additional details. Any updates to this register are applicable after Global Soft Reset.

6.5 Global Parameter Register 1

Figure 6-2. Global Parameter Register 1

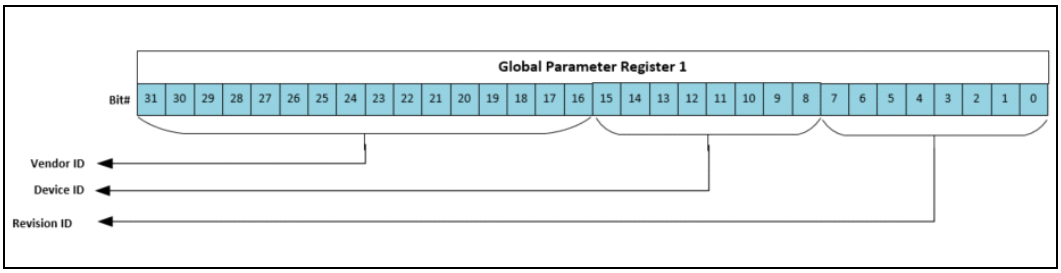


Table 6-6. Global Parameter Register 1

Bit Location	Register Description	Attributes	Description
7:0	Revision ID	RO	The Device ID, in conjunction with the Vendor ID and Revision ID, are used as one mechanism for the SW to determine which driver should be loaded.
15:8	Device ID	RO	The Device ID is allocated by the Device Vendor and identifies a particular function.
31:16	Vendor ID	RO	This identifies the Manufacturer of the Fucntion. Must be allocated by PCI-SIG.

6.6 Physical Pseudo Port x Common Parameter Register

Figure 6-3.

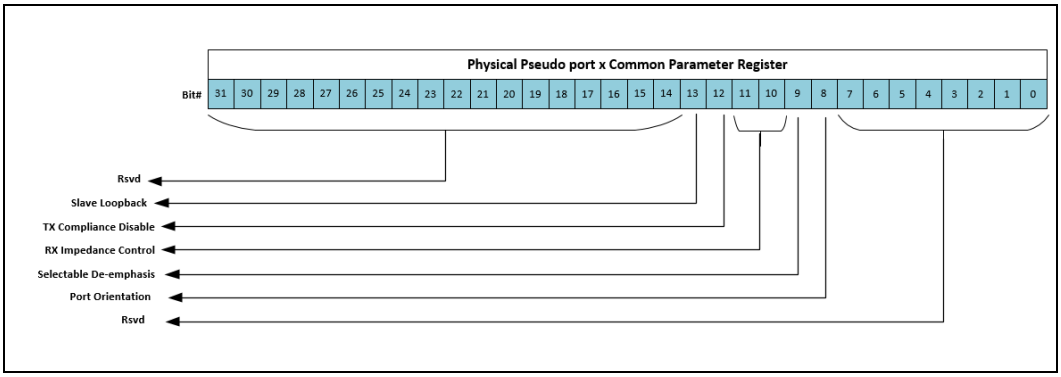


Table 6-7. Physical Pseudo Port x Common Parameter Register

Bit Location	Register Description	Attributes	Description
7:0	Rsvd	RO	Reserved for future use
8	**Port Orientation** (valid when Port Orientation Method in Global Parameter Register=0) 0: Upstream 1: Downstream (Def)	RW	This is applicable only when the Port Orientation Method is configured for static determination.

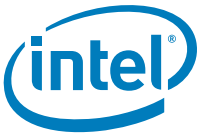


Table 6-7. Physical Pseudo Port x Common Parameter Register (Continued)

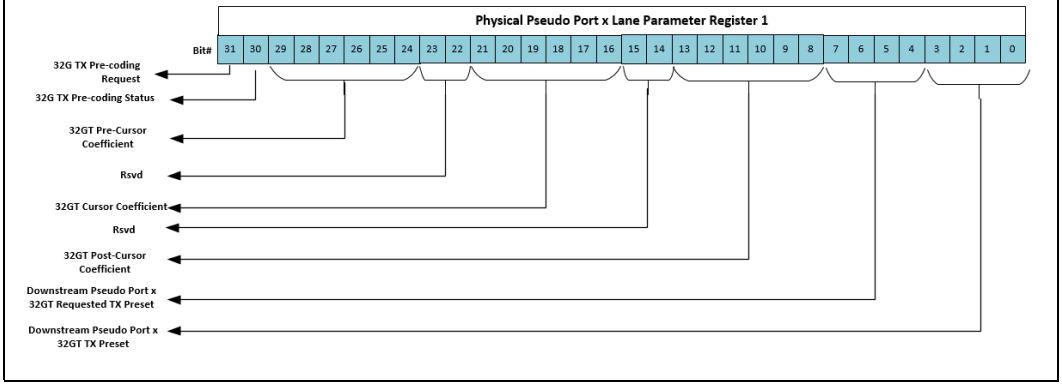
Bit Location	Register Description	Attributes	Description
9	**Selectable De-emphasis** (valid when port x Orientation=1 and Link Data Rate=5G) 0: -3.5 dB (Def) 1: -6.0 dB	RW	When the Downstream Pseudo Port is operating at 5.0 GT/s this controls the transmit de-emphasis of the Link to either -3.5 dB or -6 dB in specific situations and the value of the Selectable De-emphasis field in training sets transmitted by the Downstream Pseudo Port. Any change to this register takes effect after applying the Soft Reset for the appropriate port.
11:10	**RX Impedance Control** 00: Static- On 01: Static- Off 10: Dynamic (Def) 11: Rsvd	RW	This controls whether the Retimer dynamically applies and removes 50 ? terminations or statically has 50 ? terminations present. Any change to this resgister takes effect after applying the Soft Reset for the appropriate port.
12	TX Compliance Disable 1: Disable 0: Enable (Def)	RW	This controls whether the Retimer transmits the Compliance Pattern in the CompLoadBoard.Pattern state. Any change to this resgister takes effect after applying the Soft Reset for the appropriate port.
13	Pseudo Slave Loopback 1: Enable 0: Disable (Def)	RW	This controls whether the Retimer operates in a Forwarding mode during loopback on the Link or enters Slave Loopback on the Pseudo Port. Any change to this resgister takes effect after applying the Soft Reset for the appropriate port.
31:14	Rsvd	RO	Reserved for future use

6.7 Physical Pseudo Port x Lane Parameter Register 0

This register is reserved for future use.

6.8 Physical Pseudo Port x Lane Parameter Register 1

Figure 6-4. Physical Pseudo Port x Lane Parameter Register 1



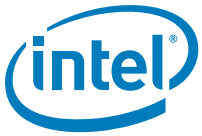


Table 6-8. Physical Pseudo Port x Lane Parameter Register 1

Bit Location	Register Description	Attributes	Description
3:0	**Downstream Pseudo Port x 32GT TX Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW	This controls the initial TX preset used by the Downstream Pseudo Port transmitter for 32.0 GT/s transmission. Any changes to this resgister takes effect after applying the Soft Reset for the appropriate port.
7:4	**Downstream Pseudo Port x 32GT Requested TX Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW	This controls the initial transmitter preset value used in the 128b/130b EQ TS2 Ordered Sets transmitted by the Downstream Pseudo Port for use at 32.0 GT/s. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.
13:8	**32G Post-Cursor Coefficient**	RW	This controls the initial TX EQ Post-Cursor used by the Downstream Pseudo Port transmitter for 32.0 GT/s transmission. This parameter provides granularity over specifying Presets using bits 3:0.
14	**Use_Preset** 1: Use Preset 0: Use Coefficients	RW	This bit indicates whether the Retimer is required to implement TX EQ based on Preset or Coefficient.
15	**Rsvd**	RO	Reserved for future use.
21:16	**32G Cursor Coefficient**	RW	This controls the initial TX EQ Cursor used by the Downstream Pseudo Port transmitter for 32.0 GT/s transmission. This parameter provides granularity over specifying Presets using bits 3:0. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.
23:22	**Rsvd**	RO	Reserved for future use.

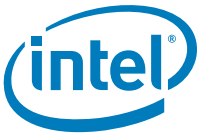


Table 6-8. Physical Pseudo Port x Lane Parameter Register 1 (Continued)

Bit Location	Register Description	Attributes	Description
29:24	**32G Pre-Cursor**	RW	This controls the initial TX EQ Pre-Cursor used by the Downstream Pseudo Port transmitter for 32.0 GT/s transmission. This parameter provides granularity over specifying Presets using bits 3:0. Any changes to this resgister takes effect after applying the Soft Reset for the appropriate port.
30	**32G TX Pre-coding Status**	RO	Status bit indicates whether this Pseudo Port has enabled Transmit precoding due to Link partner request.
31	**32G TX Pre-coding Request**	RW	This affects whether this Pseudo Port requests it's Link partner to enable Transmit precoding or not. Any changes to this resister takes effect after applying the Soft Reset for the appropriate port.

6.9 Physical Pseudo Port x Lane Parameter Register 2

Figure 6-5. Physical Pseudo Port x Lane Parameter Register 2

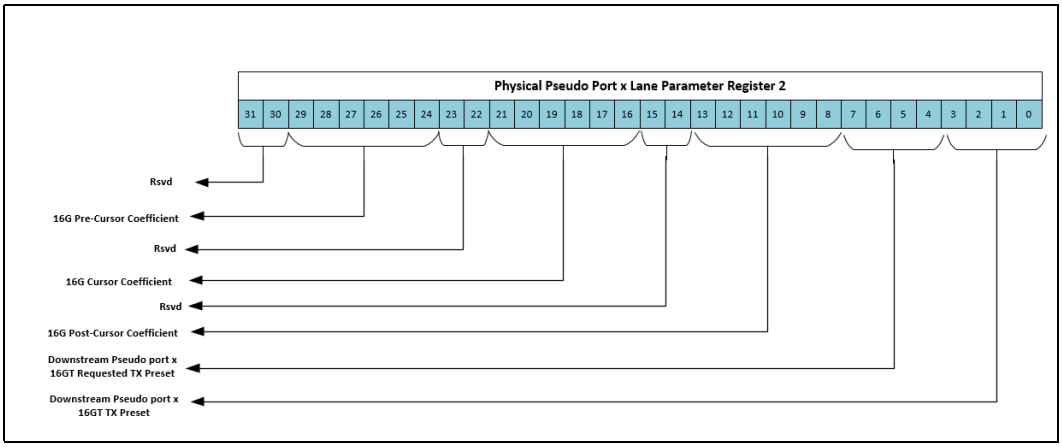


Table 6-9. Physical Pseudo Port x Lane Parameter Register 2

Bit Location	Register Description	Attributes	Description
3:0	**Downstream Pseudo Port x 16GT TX Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW	This controls the initial TX preset used by the Downstream Pseudo Port transmitter for 16.0 GT/s transmission. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.

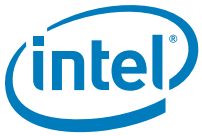


Table 6-9. Physical Pseudo Port x Lane Parameter Register 2 (Continued)

Bit Location	Register Description	Attributes	Description
7:4	**Downstream Pseudo Port x 16GT Requested TX Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW	This controls the initial transmitter preset value used in the 128b/130b EQ TS2 Ordered Sets transmitted by the Downstream Pseudo Port for use at 16.0 GT/s. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.
13:8	**16G Post-Cursor Coefficient**	RW	This controls the initial TX EQ Post-Cursor used by the Downstream Pseudo Port transmitter for 16.0 GT/s transmission. This parameter provides granularity over specifying Presets using bits 3:0. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.
14	**Use_Preset** 1: Use Preset 0: Use Coefficients	RW	This bit indicates whether the Retimer is required to implement TX EQ based on Preset or Coefficient.
15	**Rsvd**	RO	Reserved for future use.
21:16	**16G Cursor Coefficient**	RW	This controls the initial TX EQ Cursor used by the Downstream Pseudo Port transmitter for 16.0 GT/s transmission. This parameter provides granularity over specifying Presets using bits 3:0. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.
23:22	**Rsvd**	RO	Reserved for future use.
29:24	**16G Pre-Cursor Coefficient**	RW	This controls the initial TX EQ Pre-Cursor used by the Downstream Pseudo Port transmitter for 16.0 GT/s transmission. This parameter provides granularity over specifying Presets using bits 3:0. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.
31:30	**Rsvd**	RO	Reserved for future use.

6.10 Physical Pseudo Port x Lane Parameter Register 3

Figure 6-6. Physical Pseudo Port x Lane Parameter Register 3

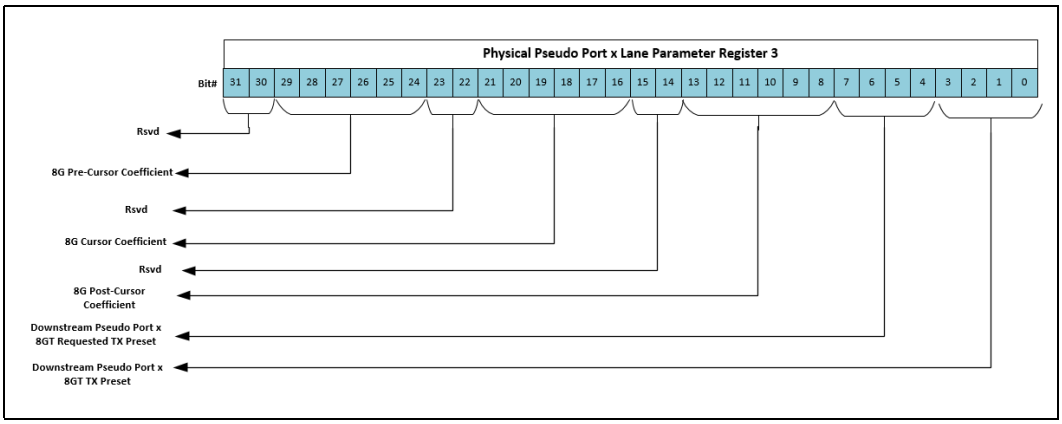


Table 6-10. Physical Pseudo Port x Lane Parameter Register 3

Bit Location	Register Description	Attributes	Description
3:0	**Downstream Pseudo Port x, 8 GT TX Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW	This controls the initial TX preset used by the Downstream Pseudo Port transmitter for 8.0 GT/s transmission. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.
7:4	**Downstream Pseudo Port x 8GT Requested TX Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW	This controls the initial transmitter preset value used in the 128b/130b EQ TS2 Ordered Sets transmitted by the Downstream Pseudo Port for use at 8.0 GT/s. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.
13:8	**8G Post-Cursor Coefficient**	RW	This controls the initial TX EQ Post-Cursor used by the Downstream Pseudo Port transmitter for 8.0 GT/s transmission. This parameter provides granularity over specifying Presets using bits 3:0.
14	**Use_Preset** 1: Use Preset 0: Use Coefficients	RW	This bit indicates whether the Retimer is required to implement TX EQ based on Preset or Coefficient.

Table 6-10. Physical Pseudo Port x Lane Parameter Register 3

Bit Location	Register Description	Attributes	Description
15	**Rsvd**	RO	Reserved for future use.
21:16	**8G Cursor Coefficient**	RW	This controls the initial TX EQ Cursor used by the Downstream Pseudo Port transmitter for 8.0 GT/s transmission. This parameter provides granularity over specifying Presets using bits 3:0. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.
23:22	**Rsvd**	RO	Reserved for future use.
29:24	**8G Pre-Cursor Coefficient**	RW	This controls the initial TX EQ Pre-Cursor used by the Downstream Pseudo Port transmitter for 8.0 GT/s transmission. This parameter provides granularity over specifying Presets using bits 3:0. Any changes to this register takes effect after applying the Soft Reset for the appropriate port.
31:30	**Rsvd**	RO	Reserved for future use.

6.11 Reset Register

Figure 6-7. Reset Register

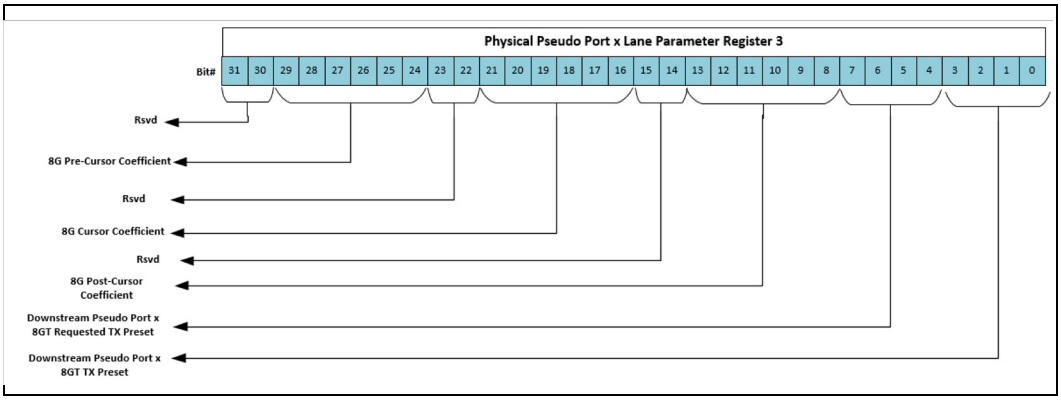


Table 6-11. Reset Register

Bit Location	Register Description	Attributes	Description
0	Soft Reset Sublink divided Port 1	RW	This bit resets the upstream and downstream links for the Sublink Port1.
1	Soft Reset Sublink divided Port 2	RW	This bit resets the upstream and downstream links for the Sublink Port2.
2	Soft Reset Sublink divided Port 3	RW	This bit resets the upstream and downstream links for the Sublink Port3.
3	Soft Reset Sublink divided Port 4	RW	This bit resets the upstream and downstream links for the Sublink Port4.
4	Soft Reset Sublink divided Port 5	RW	This bit resets the upstream and downstream links for the Sublink Port5.
5	Soft Reset Sublink divided Port 6	RW	This bit resets the upstream and downstream links for the Sublink Port6.

Table 6-11. Reset Register

Bit Location	Register Description	Attributes	Description
6	Soft Reset Sublink divided Port 7	RW	This bit resets the upstream and downstream links for the Sublink Port7.
7	Soft Reset Sublink divided Port 8	RW	This bit resets the upstream and downstream links for the Sublink Port8.
8	Global Soft reset	RW	This bit resets all the upsteam and downstream links including all sublinks. This Reset maintains the values of the defined sticky bits. This bit can be asserted by the Retimer or the system SW.
31:9	Reserved	RW	This bit resets the upstream and downstream links for the Sublink Port1.

6.12 Global Interrupt and Mask Register

Figure 6-8. Global Interrupt and Mask Register

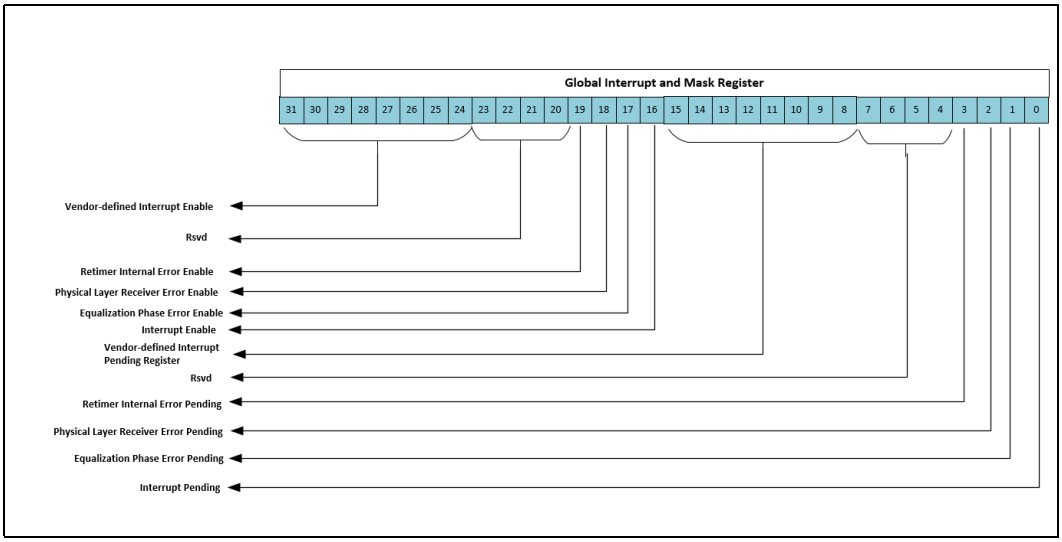


Table 6-12. Global Interrupt and Mask Register

Bit Location	Register Description	Attributes	Default	Description
0	Interrupt Pending	RO	0b	OR'd of all bits in Global Interrupt Register. When set, the INTERRUPT pin will be toggeled active if applicable.
1	Equalization Phase Error Pending	RO	0b	OR'd of all the bits in Tx EQ Phase Registers (for all subdivided links , all link speeds, all pseudo ports).
2	Physical Layer Receiver Error Pending	RO	0b	OR'd of all the bits in Receiver Error Registers (for all subdivided links and all pseudo ports).
3	Retimer Internal Error Pending	RO	0b	OR'd of all the bits in Global Retimer Internal Error Register.
7:4	Rsvd	RO	0b	Reserved for future use

Table 6-12. Global Interrupt and Mask Register

Bit Location	Register Description	Attributes	Default	Description
15:8	Vendor-defined Interrupt Pending	RO	0b	OR'd of all Vendor-defined interrupt Status bits (for all subdivided links and all pseudo ports).
16	Interrupt Enable	RW	0b	Enable bit for Interrupt Pending
17	Equalization Phase Error Enable	RW	0b	Enable bit for Equalization Phase Error Pending.
18	Physical Layer Receiver Error Enable	RW	0b	Enable bit for Physical Layer Receiver Error Pending.
19	Retimer Internal Error Enable	RW	0b	Enable bit for Retimer Internal Error Pending.
23:20	Rsvd	RO	0b	Reserved for future use
31:24	Vendor-defined Interrupt Enable	RW	0b	Enable bit for Vendor-defined Interrupt Pending.

6.13 Global Retimer Internal Interrupt and Mask Register

Figure 6-9. Global Retimer Internal Interrupt and Mask Register

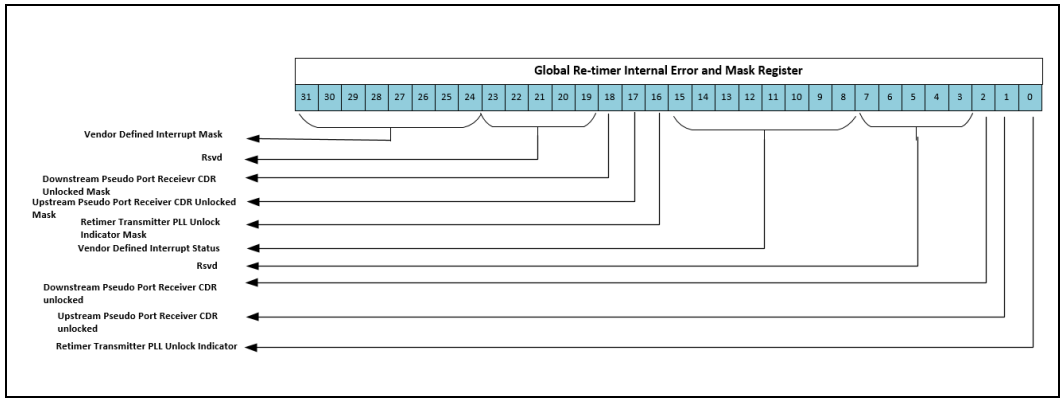


Table 6-13. Global Retimer Internal Error and Mask Register

Bit Location	Register Description	Attributes	Default	Description
0	Retimer Transmitter PLL Unlock Indicator	RW1C	0b	This bit is set whenever the Retimer upstream and/or downstream Transmitter PLLs become unlocked, and it remains set until a '1' is written, at which point this bit is cleared. This bit is the OR of both the pseudo ports' Transmitter PLL unlock statuses.
1	Upstream Pseudo Port Receiver CDR Unlocked	RW1C	0b	This bit is set whenever the Upstream Pseudo Port Receiver CDR becomes unlocked, and it remains set until a '1' is written, at which point this bit is cleared.
2	Downstream Pseudo Port Receievr CDR Unlocked	RW1C	0b	This bit is set whenever the Downstream Pseudo Port Receiver CDR becomes unlocked, and it remains set until a '1' is written, at which point this bit is cleared.
7:3	Rsvd	RO	0b	Reserved for future use

Table 6-13. Global Retimer Internal Error and Mask Register

Bit Location	Register Description	Attributes	Default	Description
15:8	Vendor Defined Interrupt Status	RW1C	0b	Vendor-defined Retimer internal error relevant interrupts.
16	Retimer Transmitter PLL Unlock Indicator Mask	RW	0b	Mask for the Retimer Transmitter PLL Unlock Indicator bit.
17	Upstream Pseudo Port Receiver CDR Unlocked Mask	RW	0b	Mask for the Upstream Pseudo Port Receiver CDR Unlocked bit.
18	Downstream Pseudo Port Receievr CDR Unlocked Mask	RW	0b	Mask for the Downstream Pseudo Port Receievr CDR Unlocked bit.
23:19	Rsvd	RO	0b	Reserved for future use
31:24	Vendor Defined Interrupt Mask	RW	0b	Mask for the Vendor-defined Interrupt Status in this register, bits (15:8).

6.14 Physical Pseudo Port x State Indicator and Mask Register

Figure 6-10. Physical Pseudo Port x State indicator and Mask Register

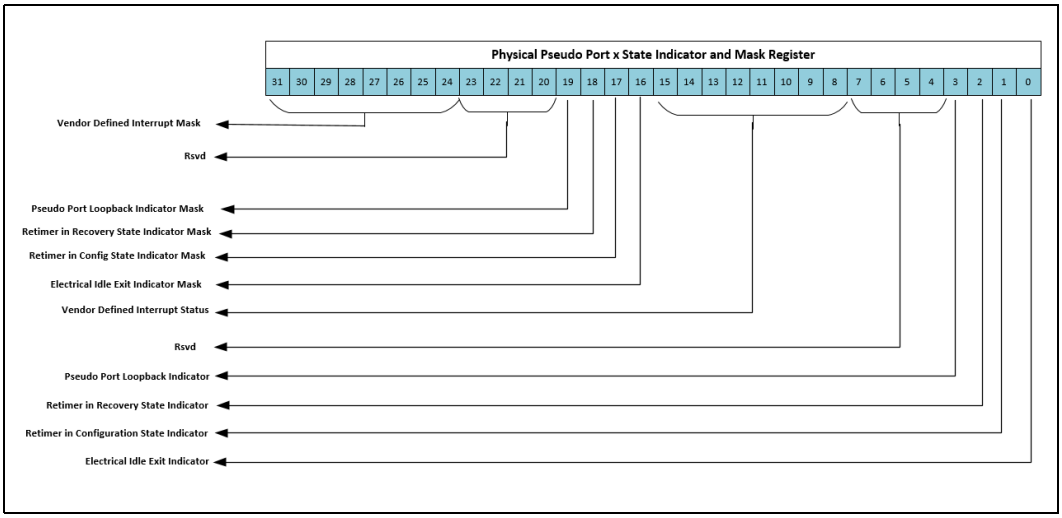


Table 6-14. Physical Pseudo Port x State Indicator and Mask Register

Bit Location	Register Description	Attributes	Default	Description
0	Electrical Idle Exit Indicator	RW1C	0b	This bit is set when the Pseudo Port x is in Electrical Idle Exit state.
1	Retimer in Configuration State Indicator	RW1C	0b	This bit is set when the Pseudo Port x is in Configuration state.
2	Retimer in Recovery State Indicator	RW1C	0b	This bit is set when the Pseudo Port x is in Recovery state.
3	Pseudo Port Loopback Indicator	RW1C	0b	This bit is set when the Pseudo Port x is in loopback state.
7:4	Rsvd	RO	0b	Reserved for future use

Table 6-14. Physical Pseudo Port x State Indicator and Mask Register

Bit Location	Register Description	Attributes	Default	Description
15:8	Vendor Defined Interrupt Status	RW1C	0b	Vendor-defined PCIe link initialization and training related interrupts.
16	Electrical Idle Exit Indicator Mask	RW	0b	Mask for the Electrical Idle Exit Indicator bit.
17	Retimer in Configuration State Indicator Mask	RW	0b	Mask for the Retimer in Configuration State Indicator bit.
18	Retimer in Recovery State Indicator Mask	RW	0b	Mask for the Retimer in Recovery State Indicator bit.
19	Pseudo Port Loopback Indicator Mask	RW	0b	Mask for the Pseudo Port Loopback Indicator bit.
23:20	Rsvd	RO	0b	Reserved for future use
31:24	Vendor Defined Interrupt Mask	RW	0b	Mask for the Vendor Defined Interrupt Status in this register, bits (15:8).

6.15 Physical Pseudo Port x 32G TXEQ Ph 2 & 3 Timeout Status and Mask Register

Figure 6-11. Physical Pseudo Port x 32G TXEQ Ph 2 & 3 Timeout Status and Mask Register

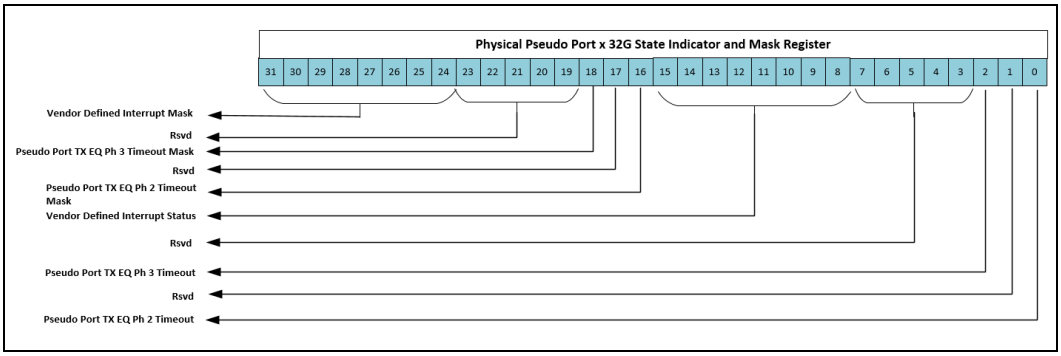


Table 6-15. Physical Pseudo Port x 32G TXEQ Ph 2 & 3 Timeout Status and Mask Register

Bit Location	Register Description	Attributes	Default	Description
0	Pseudo Port TX EQ Ph 2 Timeout	RW1C	0b	This bit is set when the Pseudo Port TX equalization phase 2 timeout is detected.
1	Rsvd	RO	0b	Reserved for future use
2	Pseudo Port TX EQ Ph 3 Timeout	RW1C	0b	This bit is set when the Pseudo Port TX equalization phase 3 timeout is detected.
7:3	Rsvd	RO	0b	Reserved for future use
15:8	Vendor Defined Interrupt Status	RW1C	0b	Vendor-defined equalization phase 2/3 related interrupts.
16	Pseudo Port TX EQ Ph 2 Timeout Mask	RW	0b	Mask for the Pseudo Port TX EQ Ph 2 Timeout error bit.
17	Rsvd	RO	0b	Reserved for future use

Table 6-15. Physical Pseudo Port x 32G TXEQ Ph 2 & 3 Timeout Status and Mask Register

Bit Location	Register Description	Attributes	Default	Description
18	Pseudo Port TX EQ Ph 3 Timeout Mask	RW	0b	Mask for the Pseudo Port TX EQ Ph 3 Timeout error bit.
23:19	Rsvd	RO	0b	Reserved for future use
31:24	Vendor Defined Interrupt Mask	RW	0b	Mask for the Vendor Defined Interrupt Status in this register, bits (15:8).

6.16 Physical Pseudo Port x16G TXEQ Ph 2 and 3 Timeout Status and Mask Register

Figure 6-12. Physical Pseudo Port x 16G TXEQ Ph 2 & 3 Timeout Status and Mask Register

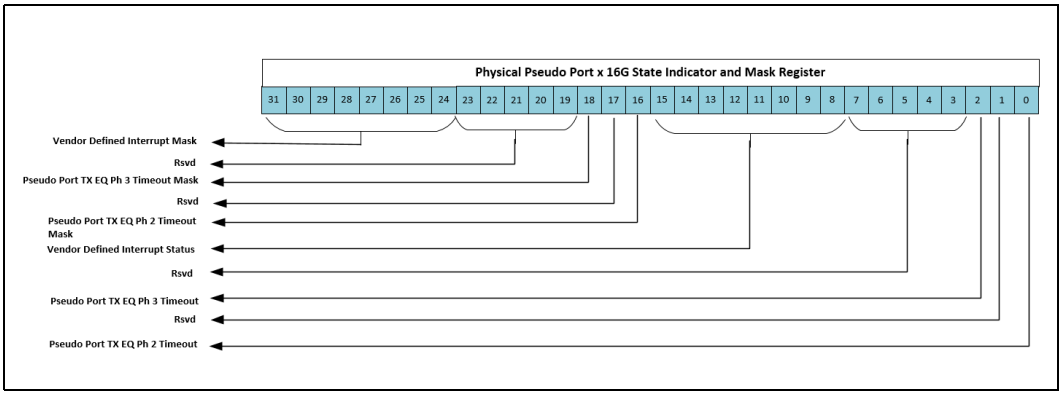


Table 6-16. Physical Pseudo Port x 16G TXEQ Ph 2 & 3 Timeout Status and Mask Register

Bit Location	Register Description	Attributes	Default	Description
0	Pseudo Port TX EQ Ph 2 Timeout	RW1C	0b	This bit is set when the Pseudo Port TX equalization phase 2 timeout is detected.
1	Rsvd	RO	0b	Reserved for future use
2	Pseudo Port TX EQ Ph 3 Timeout	RW1C	0b	This bit is set when the Pseudo Port TX equalization phase 3 timeout is detected.
7:3	Rsvd	RO	0b	Reserved for future use
15:8	Vendor Defined Interrupt Status	RW1C	0b	Vendor-defined equalization phase 2/3 related interrupts.
16	Pseudo Port TX EQ Ph 2 Timeout Mask	RW	0b	Mask for the Pseudo Port TX EQ Ph 2 Timeout error bit.
17	Rsvd	RO	0b	Reserved for future use
18	Pseudo Port TX EQ Ph 3 Timeout Mask	RW	0b	Mask for the Pseudo Port TX EQ Ph 3 Timeout error bit.
23:19	Rsvd	RO	0b	Reserved for future use
31:24	Vendor Defined Interrupt Mask	RW	0b	Mask for the Vendor Defined Interrupt Status in this register, bits (15:8).

6.17 Physical Pseudo Port x 8G TXEQ Ph 2 & 3 Timeout Status and Mask Register

Figure 6-13. Physical Pseudo Port x 8G TXEQ Ph 2 & 3 Timeout Status and Mask Register

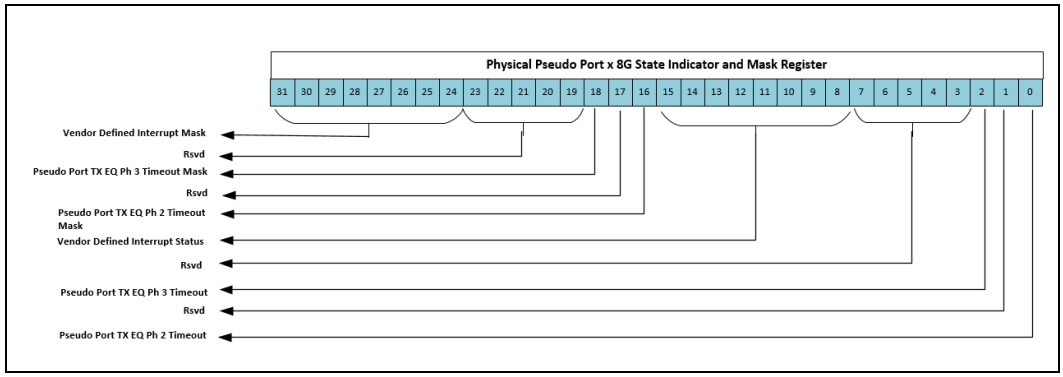


Table 6-17. Physical Pseudo Port x 8G TXEQ Ph 2 & 3 Timeout Status and Mask Register

Bit Location	Register Description	Attributes	Default	Description
0	Pseudo Port TX EQ Ph 2 Timeout	RW1C	0b	This bit is set when the Pseudo Port TX equalization phase 2 timeout is detected.
1	Rsvd	RO	0b	Reserved for future use
2	Pseudo Port TX EQ Ph 3 Timeout	RW1C	0b	This bit is set when the Pseudo Port TX equalization phase 3 timeout is detected.
7:3	Rsvd	RO	0b	Reserved for future use
15:8	Vendor Defined Interrupt Status	RW1C	0b	Vendor-defined equalization phase 2/3 related interrupts.
16	Pseudo Port TX EQ Ph 2 Timeout Mask	RW	0b	Mask for the Pseudo Port TX EQ Ph 2 Timeout error bit.
17	Rsvd	RO	0b	Reserved for future use
18	Pseudo Port TX EQ Ph 3 Timeout Mask	RW	0b	Mask for the Pseudo Port TX EQ Ph 3 Timeout error bit.
23:19	Rsvd	RO	0b	Reserved for future use
31:24	Vendor Defined Interrupt Mask	RW	0b	Mask for the Vendor Defined Interrupt Status in this register, bits (15:8).

6.18 Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register

Figure 6-14. Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register

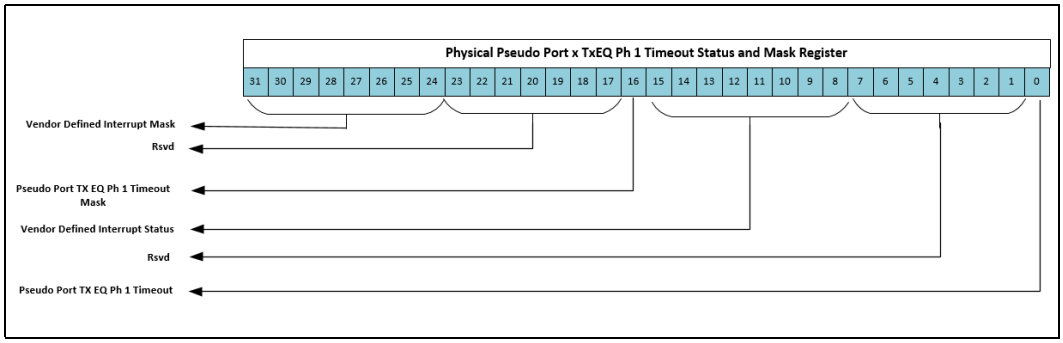
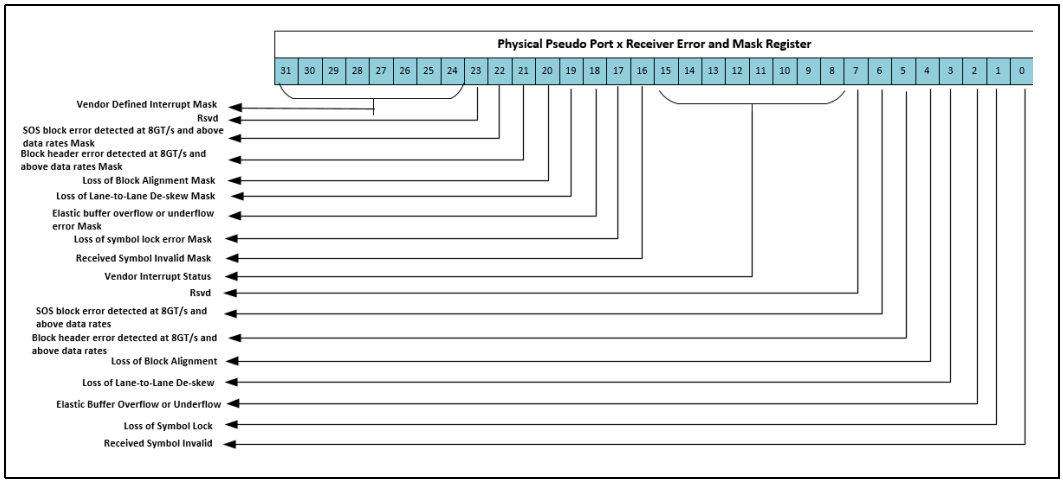


Table 6-18. Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register

Bit Location	Register Description	Attributes	Default	Description
0	Pseudo Port TX EQ Ph 1 Timeout	RW1C	0b	This bit is set when Pseudo Port TX EQ Phase 1 timeout is detected.
7:1	Rsvd	RO	0b	Reserved for future use
15:8	Vendor Defined Interrupt Status	RW1C	0b	Vendor-defined equalization phase 1 related interrupts.
16	Pseudo Port TX EQ Ph 1 Timeout Mask	RW	0b	Mask for the Pseudo Port TX EQ Ph 1 Timeout error bit.
23:17	Rsvd	RO	0b	Reserved for future use
31:24	Vendor Defined Interrupt Mask	RW	0b	Mask for the Vendor Defined Interrupt Status in this register, bits (15:8).

6.19 Physical Pseudo Port x Receiver Error and Mask Register

Figure 6-15. Physical Pseudo Port x Receiver Error and Mask Register



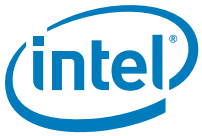


Table 6-19. Physical Pseudo Port x Receiver Error and Mask Register

Bit Location	Register Description	Attributes	Default	Description
0	Received Symbol Invalid	RW1C	0b	8b10b decode errors, running disparity errors. This bit is set if a received Symbol is found in the column corresponding to the incorrect running disparity or if the Symbol does not correspond to either column.
1	Loss of Symbol Lock	RW1C	0b	This bit is set when loss of symbol lock error is detected.
2	Elastic Buffer Overflow or Underflow	RW1C	0b	This bit is set when Elastic buffer overflow or underflow error detected.
3	Loss of Lane-to-Lane De-skew	RW1C	0b	This bit is set when loss of lane-to-lane de-skew is detected.
4	Loss of Block Alignment	RW1C	0b	This bit is set when loss of block alignment is detected on the recieiver.
5	Block header error detected at 8GT/s and above data rates	RW1C	0b	This bit is set when block header error is detected, applicable at 8GT/s and above data rates.
6	SOS block error detected at 8GT/s and above data rates	RW1C	0b	This bit is set when Skip Ordered Sets (SOS) block error is detected, applicable at 8GT/s and above data rates.
7	Rsvd	RO	0b	Reserved for future use
15:8	Vendor Defined Interrupt Status	RW1C	0b	Vendor-defined PCIe physical layer related interrupts.
16	Received Symbol Invalid Mask	RW	0b	Mask for the Received Symbol Invalid bit.
17	Loss of symbol lock error Mask	RW	0b	Mask for the Loss of Symbol Lock bit.
18	Elastic buffer overflow or underflow error Mask	RW	0b	Mask for the Elastic Buffer Overflow or Underflow error bit.
19	Loss of Lane-to-Lane De-skew Mask	RW	0b	Mask for the Loss of Lane-to-Lane De-skew error bit.
20	Loss of Block Alignment Mask	RW	0b	Mask for the Loss of Block Alignment error bit.
21	Block header error detected at 8GT/s and above data rates Mask	RW	0b	Mask for the block header error detected at 8GT/s and above data rates.
22	SOS block error detected at 8GT/s and above data rates Mask	RW	0b	Mask for the SOS block error detected at 8GT/s and above data rates.
23	Rsvd	RO	0b	Reserved for future use
31:24	Vendor Defined Interrupt Mask	RW	0b	Mask for the Vendor Defined Interrupt Status in this register, bits (15:8).

6.20 Register Offsets for Different Link Subdivision (Bifurcation)

Table 6 18 shows offsets for various registers.

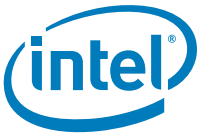


Table 6-20. Register Offsets

		Offset (dec)	Offset (hex)	Link Sub Division			
Global Parameter Register 0		0	0x0000				
Global Parameter Register 1		4	0x0004				
Global Interrupt and Mask Register		8	0x0008				
Global Re-timer Internal Error and Mask Register		12	0x000C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 0, Link Sub Divided Port 1	16	0x0010	x2	x4	x8	x16
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 0		20	0x0014				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 0		24	0x0018				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 0		28	0x001C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 0		32	0x0020				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 1		36	0x0024				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 1		40	0x0028				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 1		44	0x002C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 1		48	0x0030				
Physical Pseudo Port x State Indicator and Mask Register		52	0x0034				
Rsvd		56	0x0038				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		60	0x003C				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		64	0x0040				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		68	0x0044				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		72	0x0048				
Physical Pseudo Port x Receiver Error and Mask Register		76	0x004C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 0, Link Sub Divided Port 2	80	0x0050	x2			
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 2		84	0x0054				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 2		88	0x0058				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 2		92	0x005C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 2		96	0x0060				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 3		100	0x0064				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 3		104	0x0068				

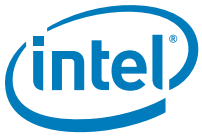


Table 6-20. Register Offsets (Continued)

		Offset (dec)	Offset (hex)	Link Sub Division			
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 3		108	0x006C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 3		112	0x0070				
Physical Pseudo Port x State Indicator and Mask Register		116	0x0074				
Rsvd		120	0x0078				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		124	0x007C				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		128	0x0080				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		132	0x0084				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		136	0x0088				
Physical Pseudo Port x Receiver Error and Mask Register		140	0x008C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 0, Link Sub Divided Port 3	144	0x0090	x2	x4		
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 4		148	0x0094				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 4		152	0x0098				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 4		156	0x009C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 4		160	0x00A0				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 5		164	0x00A4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 5		168	0x00A8				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 5		172	0x00AC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 5		176	0x00B0				
Physical Pseudo Port x State Indicator and Mask Register		180	0x00B4				
Rsvd		184	0x00B8				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		188	0x00BC				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		192	0x00C0				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		196	0x00C4				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		200	0x00C8				
Physical Pseudo Port x Receiver Error and Mask Register		204	0x00CC				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 0, Link Sub Divided Port 4	208	0x00D0	x2			
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 6		212	0x00D4				

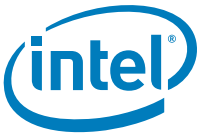


Table 6-20. Register Offsets (Continued)

		Offset (dec)	Offset (hex)	Link Sub Division			
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 6		216	0x00D8				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 6		220	0x00DC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 6		224	0x00E0				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 7		228	0x00E4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 7		232	0x00E8				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 7		236	0x00EC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 7		240	0x00F0				
Physical Pseudo Port x State Indicator and Mask Register		244	0x00F4				
Rsvd		248	0x00F8				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		252	0x00FC				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		256	0x0100				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		260	0x0104				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		264	0x0108				
Physical Pseudo Port x Receiver Error and Mask Register		268	0x010C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 0, Link Sub Divided Port 5	272	0x0110	x2	x4	x8	
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 8		276	0x0114				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 8		280	0x0118				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 8		284	0x011C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 8		288	0x0120				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 9		292	0x0124				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 9		296	0x0128				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 9		300	0x012C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 9		304	0x0130				
Physical Pseudo Port x State Indicator and Mask Register		308	0x0134				
Rsvd		312	0x0138				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		316	0x013C				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		320	0x0140				

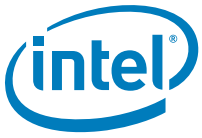


Table 6-20. Register Offsets (Continued)

		Offset (dec)	Offset (hex)	Link Sub Division			
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		324	0x0144				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		328	0x0148				
Physical Pseudo Port x Receiver Error and Mask Register		332	0x014C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 0, Link Sub Divided Port 6	336	0x0150	x2			
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 10		340	0x0154				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 10		344	0x0158				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 10		348	0x015C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 10		352	0x0160				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 11		356	0x0164				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 11		360	0x0168				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 11		364	0x016C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 11		368	0x0170				
Physical Pseudo Port x State Indicator and Mask Register		372	0x0174				
Rsvd		376	0x0178				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		380	0x017C				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		384	0x0180				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		388	0x0184				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		392	0x0188				
Physical Pseudo Port x Receiver Error and Mask Register		396	0x018C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 0, Link Sub Divided Port 7	400	0x0190	x2	x4		
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 12		404	0x0194				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 12		408	0x0198				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 12		412	0x019C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 12		416	0x01A0				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 13		420	0x01A4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 13		424	0x01A8				

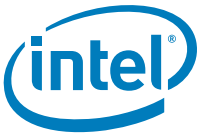


Table 6-20. Register Offsets (Continued)

		Offset (dec)	Offset (hex)	Link Sub Division			
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 13		428	0x01AC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 13		432	0x01B0				
Physical Pseudo Port x State Indicator and Mask Register		436	0x01B4				
Rsvd		440	0x01B8				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		444	0x01BC				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		448	0x01C0				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		452	0x01C4				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		456	0x01C8				
Physical Pseudo Port x Receiver Error and Mask Register		460	0x01CC				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 0, Link Sub Divided Port 8	464	0x01D0	x2			
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 14		468	0x01D4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 14		472	0x01D8				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 14		476	0x01DC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 14		480	0x01E0				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 15		484	0x01E4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 15		488	0x01E8				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 15		492	0x01EC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 15		496	0x01F0				
Physical Pseudo Port x State Indicator and Mask Register		500	0x01F4				
Rsvd		504	0x01F8				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		508	0x01FC				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		512	0x0200				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		516	0x0204				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		520	0x0208				
Physical Pseudo Port x Receiver Error and Mask Register		524	0x020C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 1, Link Sub Divided Port 1	528	0x0210	x2	x4	x8	x16
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 0		532	0x0214				

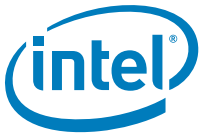


Table 6-20. Register Offsets (Continued)

		Offset (dec)	Offset (hex)	Link Sub Division			
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 0		536	0x0218				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 0		540	0x021C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 0		544	0x0220				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 1		548	0x0224				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 1		552	0x0228				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 1		556	0x022C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 1		560	0x0230				
Physical Pseudo Port x State Indicator and Mask Register		564	0x0234				
Rsvd		568	0x0238				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		572	0x023C				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		576	0x0240				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		580	0x0244				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		584	0x0248				
Physical Pseudo Port x Receiver Error and Mask Register		588	0x024C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 1, Link Sub Divided Port 2	592	0x0250	x2			
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 2		596	0x0254				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 2		600	0x0258				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 2		604	0x025C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 2		608	0x0260				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 3		612	0x0264				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 3		616	0x0268				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 3		620	0x026C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 3		624	0x0270				
Physical Pseudo Port x State Indicator and Mask Register		628	0x0274				
Rsvd		632	0x0278				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		636	0x027C				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		640	0x0280				

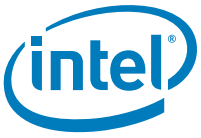


Table 6-20. Register Offsets (Continued)

		Offset (dec)	Offset (hex)	Link Sub Division			
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		644	0x0284				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		648	0x0288				
Physical Pseudo Port x Receiver Error and Mask Register		652	0x028C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 1, Link Sub Divided Port 3	656	0x0290	x2	x4		
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 4		660	0x0294				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 4		664	0x0298				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 4		668	0x029C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 4		672	0x02A0				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 5		676	0x02A4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 5		680	0x02A8				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 5		684	0x02AC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 5		688	0x02B0				
Physical Pseudo Port x State Indicator and Mask Register		692	0x02B4				
Rsvd		696	0x02B8				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		700	0x02BC				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		704	0x02C0				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		708	0x02C4				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		712	0x02C8				
Physical Pseudo Port x Receiver Error and Mask Register		716	0x02CC				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 1, Link Sub Divided Port 4	720	0x02D0	x2			
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 6		724	0x02D4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 6		728	0x02D8				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 6		732	0x02DC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 6		736	0x02E0				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 7		740	0x02E4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 7		744	0x02E8				

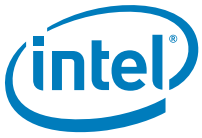


Table 6-20. Register Offsets (Continued)

		Offset (dec)	Offset (hex)	Link Sub Division			
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 7		748	0x02EC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 7		752	0x02F0				
Physical Pseudo Port x State Indicator and Mask Register		756	0x02F4				
Rsvd		760	0x02F8				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		764	0x02FC				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		768	0x0300				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		772	0x0304				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		776	0x0308				
Physical Pseudo Port x Receiver Error and Mask Register		780	0x030C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 1, Link Sub Divided Port 5	784	0x0310	x2	x4	x8	
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 8		788	0x0314				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 8		792	0x0318				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 8		796	0x031C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 8		800	0x0320				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 9		804	0x0324				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 9		808	0x0328				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 9		812	0x032C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 9		816	0x0330				
Physical Pseudo Port x State Indicator and Mask Register		820	0x0334				
Rsvd		824	0x0338				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		828	0x033C				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		832	0x0340				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		836	0x0344				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		840	0x0348				
Physical Pseudo Port x Receiver Error and Mask Register		844	0x034C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 1, Link Sub Divided Port 6	848	0x0350	x2			
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 10		852	0x0354				

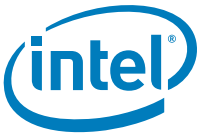


Table 6-20. Register Offsets (Continued)

		Offset (dec)	Offset (hex)	Link Sub Division			
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 10		856	0x0358				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 10		860	0x035C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 10		864	0x0360				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 11		868	0x0364				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 11		872	0x0368				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 11		876	0x036C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 11		880	0x0370				
Physical Pseudo Port x State Indicator and Mask Register		884	0x0374				
Rsvd		888	0x0378				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		892	0x037C				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		896	0x0380				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		900	0x0384				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		904	0x0388				
Physical Pseudo Port x Receiver Error and Mask Register		908	0x038C				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 1, Link Sub Divided Port 7	912	0x0390	x2	x4		
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 12		916	0x0394				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 12		920	0x0398				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 12		924	0x039C				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 12		928	0x03A0				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 13		932	0x03A4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 13		936	0x03A8				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 13		940	0x03AC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 13		944	0x03B0				
Physical Pseudo Port x State Indicator and Mask Register		948	0x03B4				
Rsvd		952	0x03B8				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		956	0x03BC				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		960	0x03C0				

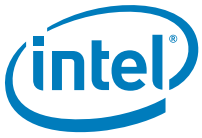


Table 6-20. Register Offsets (Continued)

		Offset (dec)	Offset (hex)	Link Sub Division			
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		964	0x03C4				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		968	0x03C8				
Physical Pseudo Port x Receiver Error and Mask Register		972	0x03CC				
Physical Pseudo Port x Common Parameter Register	x: Pseudo Port 1, Link Sub Divided Port 8	976	0x03D0	x2			
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 14		980	0x03D4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 14		984	0x03D8				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 14		988	0x03DC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 14		992	0x03E0				
Physical Pseudo Port x Lane Parameter Register 0, (Rsvd), Lane 15		996	0x03E4				
Physical Pseudo Port x Lane Parameter Register 1, (32GT), Lane 15		1000	0x03E8				
Physical Pseudo Port x Lane Parameter Register 2, (16GT), Lane 15		1004	0x03EC				
Physical Pseudo Port x Lane Parameter Register 3, (8GT), Lane 15		1008	0x03F0				
Physical Pseudo Port x State Indicator and Mask Register		1012	0x03F4				
Rsvd		1016	0x03F8				
Physical Pseudo Port x 32G TxEQ Ph 2 & 3 Timeout Status and Mask Register		1020	0x03FC				
Physical Pseudo Port x 16G TxEQ Ph 2 & 3 Timeout Status and Mask Register		1024	0x0400				
Physical Pseudo Port x 8G TxEQ Ph 2 & 3 Timeout Status and Mask Register		1028	0x0404				
Physical Pseudo Port x TxEQ Ph 1 Timeout Status and Mask Register		1032	0x0408				
Physical Pseudo Port x Receiver Error and Mask Register		1036	0x040C				

		Offset (dec)	Offset (hex)	Link Sub Division				
Rsvd		1040	0x0410					
Reset Register		1044	0x0414					Reset Register
Host Defined Register 1		1048	0x0418					See Note 1
Host Defined Register 2		1052	0x041C					See Note 1
Host Defined Register 3		1056	0x0420					See Note 1
Host Defined Register 3		1060	0x0424					
Host Defined Register 3		1064	0x0428					
Host Defined Register 3		1068	0x042C					
Host Defined Register 3		1072	0x0430					

		Offset (dec)	Offset (hex)	Link Sub Division				
Host Defined Register 3		1076	0x0434					
Host Defined Register 3		1080	0x0438					
Host Defined Register 3		1084	0x043C					
Rsvd		1088	0x0440					
Rsvd		1092	0x0444					
Rsvd		1096	0x0448					
Rsvd		1100	0x044C					
Rsvd		1104	0x0450					
Rsvd		1108	0x0454					
Rsvd		1112	0x0458					
Rsvd		1116	0x045C					
Rsvd		1120	0x0460					
Rsvd		1124	0x0464					
Rsvd		1128	0x0468					
Rsvd		1132	0x046C					
Rsvd		1136	0x0470					
Rsvd		1140	0x0474					
Rsvd		1144	0x0478					
Rsvd		1148	0x047C					
Rsvd		1152	0x0480					
Rsvd		1156	0x0484					
Rsvd		1160	0x0488					
Rsvd		1164	0x048C					
vendor Defined (See Note 2)		1168	0x0490					

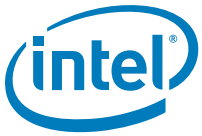
Notes:
1. 1. Usage of Host Defined Registers is implementation specific and details need to be discussed between the system vendor and the Retimer vendor.
2. 2. Offsets from 0x0490 onwards can be used for Vendor Defined purposes.

6.21 Register Mapping to Base Specification Inband Address

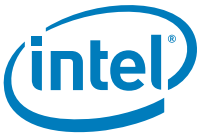
The Following table lists mapping of three Retimer registers that are indicated in the Table 6 18 to the base specification defined inband addresses.

The three registers that are mapped to the base specification defined inband address space include Host Defined Register-1, Host Defined Register-2 and Global Parameter Register 1.

This mapping makes the three Retimer registers accessible using base specification defined inband protocol.



Base Specification defined In-band Address	Mapped Address [bits] from Retimer Supplemental Specification	Description
A0	0x0418 [0:7]	Host Defined Register-1
A1	0x0418 [8:15]	Host Defined Register-1
A2	0x0418 [16:23]	Host Defined Register-1
A3	0x0418 [24:31]	Host Defined Register-1
A4	0x041C [0:7]	Host Defined Register-2
A5	0x041C [8:15]	Host Defined Register-2
A6	0x041C [16:23]	Host Defined Register-2
A7	0x041C[24:31]	Host Defined Register-2
A8	0x0004 [0:7]	Global Parameter Register-1/Revision ID
A9	0x0004 [8:15]	Global Parameter Register-1/Device ID
AA	0x0004 [16:23]	Global Parameter Register-1/Vendor ID LSB
AB	0x0004 [24:31]	Global Parameter Register-1/Vendor ID MSB
AC	0x0420 [31:0]	Host Defined Register-3 Egress Lane for Lane 3 DFPP[31:28] Egress Lane for Lane 3 UFPP[27:24] Egress Lane for Lane 2 DFPP[23:20] Egress Lane for Lane 2 UFPP[19:16] Egress Lane for Lane 1 DFPP[15:12] Egress Lane for Lane 1 UFPP[11:8] Egress Lane for Lane 0 DFPP[7:4] Egress Lane for Lane 0 UFPP[3:0]
AD	0x0424 [31:0]	Host Defined Register-3 Egress Lane for Lane 7 DFPP[31:28] Egress Lane for Lane 7 UFPP[27:24] Egress Lane for Lane 6 DFPP[23:20] Egress Lane for Lane 6 UFPP[19:16] Egress Lane for Lane 5 DFPP[15:12] Egress Lane for Lane 5 UFPP[11:8] Egress Lane for Lane 4 DFPP[7:4] Egress Lane for Lane 4 UFPP[3:0]
AE	0x0428 [31:0]	Host Defined Register-3 Egress Lane for Lane 11 DFPP[31:28] Egress Lane for Lane 11 UFPP[27:24] Egress Lane for Lane 10 DFPP[23:20] Egress Lane for Lane 10 UFPP[19:16] Egress Lane for Lane 9 DFPP[15:12] Egress Lane for Lane 9 UFPP[11:8] Egress Lane for Lane 8 DFPP[7:4] Egress Lane for Lane 8 UFPP[3:0]
AF	0x042C [31:0]	Host Defined Register-3 Egress Lane for Lane 15 DFPP[31:28] Egress Lane for Lane 15 UFPP[27:24] Egress Lane for Lane 14 DFPP[23:20] Egress Lane for Lane 14 UFPP[19:16] Egress Lane for Lane 13 DFPP[15:12] Egress Lane for Lane 13 UFPP[11:8] Egress Lane for Lane 12 DFPP[7:4] Egress Lane for Lane 12 UFPP[3:0]



Base Specification defined In-band Address	Mapped Address [bits] from Retimer Supplemental Specification	Description
B0	0x0430 [31:0]	Host Defined Register-4 Egress Deskew latency Lane 3[31:28] Egress Deskew latency Lane 2[27:24] Egress Deskew latency Lane 1[23:20] Egress Deskew latency Lane 0[19:16] Ingress Deskew latency Lane 3[15:12] Ingress Deskew latency Lane 2[11:8] Ingress Deskew latency Lane 1[7:4] Ingress Deskew latency Lane 0[3:0]
B1	0x0434 [31:0]	Host Defined Register-4 Egress Deskew latency Lane 7[31:28] Egress Deskew latency Lane 6[27:24] Egress Deskew latency Lane 5[23:20] Egress Deskew latency Lane 4[19:16] Ingress Deskew latency Lane 7[15:12] Ingress Deskew latency Lane 6[11:8] Ingress Deskew latency Lane 5[7:4] Ingress Deskew latency Lane 4[3:0]
B2	0x0438 [31:0]	Host Defined Register-4 Egress Deskew latency Lane 11[31:28] Egress Deskew latency Lane 10[27:24] Egress Deskew latency Lane 9[23:20] Egress Deskew latency Lane 8[19:16] Ingress Deskew latency Lane 11[15:12] Ingress Deskew latency Lane 10[11:8] Ingress Deskew latency Lane 9[7:4] Ingress Deskew latency Lane 8[3:0]
B3	0x043C [31:0]	Host Defined Register-4 Egress Deskew latency Lane 15[31:28] Egress Deskew latency Lane 14[27:24] Egress Deskew latency Lane 13[23:20] Egress Deskew latency Lane 12[19:16] Ingress Deskew latency Lane 15[15:12] Ingress Deskew latency Lane 14[11:8] Ingress Deskew latency Lane 13[7:4] Ingress Deskew latency Lane 12[3:0]

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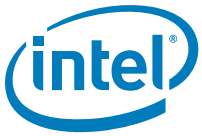

7 Annex

7.1 Pin List for x16 Pinout

Table 7-1. Pin List for x16 Pinout

	Pin Number	Pin Signal
1.	FD1	GND
2.	ET1	GND
3.	EJ1	GND
4.	EB1	GND
5.	DR1	GND
6.	DH1	GND
7.	DA1	GND
8.	CP1	GND
9.	CG1	GND
10.	BY1	GND
11.	BN1	GND
12.	BF1	GND
13.	AW1	GND
14.	AM1	GND
15.	AE1	GND
16.	V1	GND
17.	L1	GND
18.	FB2	GND
19.	ER2	GND
20.	EH2	GND
21	EA2	GND
22.	DP2	GND
23.	DG2	GND
24.	CY2	GND
25.	CN2	GND
26.	CF2	GND
27.	BW2	GND
28.	BM2	GND
29.	BE2	GND
30.	AV2	GND
31.	AL2	GND
32.	AD2	GND
33.	U2	GND
34.	K2	GND
35.	FC3	GND

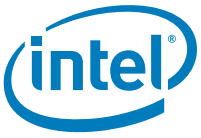

Table 7-1. Pin List for x16 Pinout

	Pin Number	Pin Signal
36.	EP4	GND
37.	EG4	GND
38.	DY4	GND
39.	DN4	GND
40.	DF4	GND
41.	CW4	GND
42.	CM4	GND
43.	CE4	GND
44.	BV4	GND
45.	BL4	GND
46.	BD4	GND
47.	AU4	GND
48.	AK4	GND
49.	AC4	GND
50.	T4	GND
51.	J4	GND
52.	FC6	GND
53.	FC9	GND
54.	FJ12	GND
55.	FA15	GND
56.	EP13	GND
57.	EG13	GND
58.	DY13	GND
59.	DN13	GND
60.	DF13	GND
61.	CW13	GND
62.	CM13	GND
63.	CE13	GND
64.	BV13	GND
65.	BL13	GND
66.	BD13	GND
67.	AU13	GND
68.	AK13	GND
69.	AC13	GND
70.	T13	GND
71.	EP22	GND
72.	EG22	GND
73.	DY22	GND
74.	DN22	GND
75.	DF22	GND
76.	CW22	GND
77.	CM22	GND

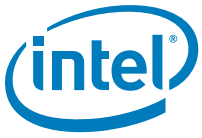

Table 7-1. Pin List for x16 Pinout

	Pin Number	Pin Signal
78.	CE22	GND
79.	BV22	GND
80.	BL22	GND
81.	BD22	GND
82.	AU22	GND
83.	AK22	GND
84.	AC22	GND
85.	T22	GND
86.	J22	GND
87.	FF14	GND
88.	FJ19	GND
89.	FF21	GND
90.	FC19	GND
91.	FC23	GND
92.	FC25	GND
93.	FC28	GND
94.	FA32	GND
95.	EP32	GND
96.	EG32	GND
97.	DY32	GND
98.	DN32	GND
99.	DF32	GND
100.	CW32	GND
101.	CM32	GND
102	CE32	GND
103.	BV32	GND
104.	BL32	GND
105.	BD32	GND
106.	AU32	GND
107.	AK32	GND
108.	AC32	GND
109.	T32	GND
110.	E14	GND
111.	H12	GND
112.	H16	GND
113.	H19	GND
114.	B19	GND
115.	H31	GND
116.	E27	GND
117.	E30	GND
118.	E33	GND
119.	FB34	GND

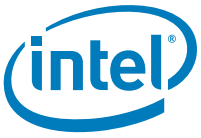

Table 7-1. Pin List for x16 Pinout

	Pin Number	Pin Signal
120.	ER34	GND
121.	EH34	GND
122.	EA34	GND
123.	DP34	GND
124.	DG34	GND
125.	CY34	GND
126.	CN34	GND
127.	CF34	GND
128.	BW34	GND
129.	BM34	GND
130.	BE34	GND
131.	AV34	GND
132.	AL34	GND
133.	AD34	GND
134.	U34	GND
135.	K34	GND
136.	FD35	GND
137.	ET35	GND
138.	EJ35	GND
139.	EB35	GND
140.	DR35	GND
141.	DH35	GND
142.	DA35	GND
143.	CP35	GND
144.	CG35	GND
145.	BY35	GND
146.	BN35	GND
147.	BF35	GND
148.	AW35	GND
149.	AM35	GND
150.	AE35	GND
151.	V35	GND
152.	L35	GND
153.	CM17	VD_PWR
154.	CM20	VD_PWR
155.	CE17	VD_PWR
156.	CE20	VD_PWR
157.	BV17	VD_PWR
158.	BV20	VD_PWR
159.	EP17	VD_PWR
160.	EP20	VD_PWR
161.	EG17	VD_PWR

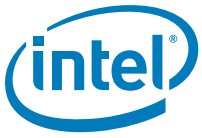

Table 7-1. Pin List for x16 Pinout

	Pin Number	Pin Signal
162.	EG20	VD_PWR
163.	DY17	VD_PWR
164.	DY20	VD_PWR
165.	DN17	VD_PWR
166.	DN20	VD_PWR
167.	DF17	VD_PWR
168.	DF20	VD_PWR
169.	CW17	VD_PWR
170.	CW20	VD_PWR
171.	BL17	VD_PWR
172.	BL20	VD_PWR
173.	BD17	VD_PWR
174.	BD20	VD_PWR
175.	AU17	VD_PWR
176.	AU20	VD_PWR
177.	AK17	VD_PWR
178.	AK20	VD_PWR
179.	AC17	VD_PWR
180.	AC20	VD_PWR
181.	T17	VD_PWR
182.	T20	VD_PWR
183.	M26	A_PETp0
184.	P29	A_PETn0
185.	W26	A_PETp1
186.	AA29	A_PETn1
187.	AF26	A_PETp2
188.	AH29	A_PETn2
189.	AN26	A_PETp3
190.	AR29	A_PETn3
191.	AY26	A_PETp4
192.	BB29	A_PETn4
193.	BG26	A_PETp5
194.	BJ29	A_PETn5
195.	BP26	A_PETp6
196.	BT29	A_PETn6
197.	CA26	A_PETp7
198.	CC29	A_PETn7
199.	CH26	A_PETp8
200.	CK29	A_PETn8
201.	CR26	A_PETp9
202.	CU29	A_PETn9
203.	DB26	A_PETp10

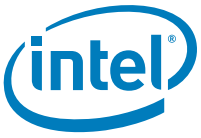

Table 7-1. Pin List for x16 Pinout

	Pin Number	Pin Signal
204.	DD29	A_PETn10
205.	DJ26	A_PETp11
206.	DL29	A_PETn11
207.	DT26	A_PETp12
208.	DV29	A_PETn12
209.	EC26	A_PETp13
210.	EE29	A_PETn13
211.	EK26	A_PETp14
212.	EM29	A_PETn14
213.	EU26	A_PETp15
214.	EW29	A_PETn15
215.	N34	B_PERp0
216.	R35	B_PERn0
217.	Y34	B_PERp1
218.	AB35	B_PERn1
219.	AG34	B_PERp2
220.	AJ35	B_PERn2
221.	AP34	B_PERp3
222.	AT35	B_PERn3
223.	BA34	B_PERp4
224.	BC35	B_PERn4
225.	BH34	B_PERp5
226.	BK35	B_PERn5
227.	BR34	B_PERp6
228.	BU35	B_PERn6
229.	CB34	B_PERp7
230.	CD35	B_PERn7
231.	CJ34	B_PERp8
232.	CL35	B_PERn8
233.	CT34	B_PERp9
234.	CV35	B_PERn9
235.	DC34	B_PERp10
236.	DE35	B_PERn10
237.	DK34	B_PERp11
238.	DM35	B_PERn11
239.	DU34	B_PERp12
240.	DW35	B_PERn12
241.	ED34	B_PERp13
242.	EF35	B_PERn13
243.	EL34	B_PERp14
244.	EN35	B_PERn14
245.	EV34	B_PERp15

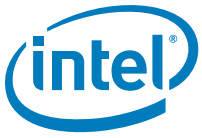

Table 7-1. Pin List for x16 Pinout

	Pin Number	Pin Signal
246.	EY35	B_PERn15
247.	R1	A_PERp0
248.	N2	A_PERn0
249.	AB1	A_PERp1
250.	Y2	A_PERn1
251.	AJ1	A_PERp2
252.	AG2	A_PERn2
253.	AT1	A_PERp3
254.	AP2	A_PERn3
255.	BC1	A_PERp4
256.	BA2	A_PERn4
257.	BK1	A_PERp5
258.	BH2	A_PERn5
259.	BU1	A_PERp6
260.	BR2	A_PERn6
261.	CD1	A_PERp7
262.	CB2	A_PERn7
263.	CL1	A_PERp8
264.	CJ2	A_PERn8
265.	CV1	A_PERp9
266.	CT2	A_PERn9
267.	DE1	A_PERp10
268.	DC2	A_PERn10
269.	DM1	A_PERp11
270.	DK2	A_PERn11
271.	DW1	A_PERp12
272.	DU2	A_PERn12
273.	EF1	A_PERp13
274.	ED2	A_PERn13
275.	EN1	A_PERp14
276.	EL2	A_PERn14
277.	EY1	A_PERp15
278.	EV2	A_PERn15
279.	M7	B_PETp0
280.	P10	B_PETn0
281.	W7	B_PETp1
282.	AA10	B_PETn1
283.	AF7	B_PETp2
284.	AH10	B_PETn2
285.	AN7	B_PETp3
286.	AR10	B_PETn3
287.	AY7	B_PETp4

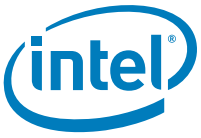

Table 7-1. Pin List for x16 Pinout

	Pin Number	Pin Signal
288.	BB10	B_PETn4
289.	BG7	B_PETp5
290.	BJ10	B_PETn5
291.	BP7	B_PETp6
292.	BT10	B_PETn6
293.	CA7	B_PETp7
294.	CC10	B_PETn7
295.	CH7	B_PETp8
296.	CK10	B_PETn8
297.	CR7	B_PETp9
298.	CU10	B_PETn9
299.	DB7	B_PETp10
300.	DD10	B_PETn10
301.	DJ7	B_PETp11
302.	DL10	B_PETn11
303.	DT7	B_PETp12
304.	DV10	B_PETn12
305.	EC7	B_PETp13
306.	EE10	B_PETn13
307.	EK7	B_PETp14
308.	EM10	B_PETn14
309.	EU7	B_PETp15
310.	EW10	B_PETn15
311.	FJ16	REFCLK+
312.	FF18	REFCLK-
313.	B16	REFCLK_Out+
314.	E18	REFCLK_Out-
315.	F2	PERST#
316.	G35	CLKREQ#
317.	B6	JTAG_TDI
318.	B9	JTAG_TDO
319.	B12	JTAG_TMS
320.	B3	JTAG_TCK
321.	E8	JTAG_TRST#
322.	B31	SMBCLK
323.	B28	SMBDAT
324.	F34	SMB_ADDR_1
325.	B23	SMB_ADDR_2
326.	B25	SMB_ADDR_3/VD_16
327.	FJ3	EE_DAT/VD_7
328.	FF5	EE_CLK/VD_8
329.	FJ23	VD_1

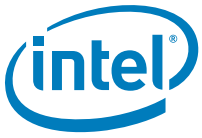

Table 7-1. Pin List for x16 Pinout

	Pin Number	Pin Signal
330.	FF24	VD_2
331.	FJ6	VD_3
332.	FF8	VD_4
333.	FJ9	VD_5
334.	FF11	VD_6
335.	FJ25	VD_9
336.	FF27	VD_10
337.	FJ28	VD_11
338.	FF30	VD_12
339.	FJ31	VD_13
340.	FF33	VD_14
341.	G1	VD_15
342	E11	RX_DET_BYP
343.	FG1	NCTF
344.	FH2	NCTF
345.	FE2	NCTF
346.	D1	NCTF
347.	A1	NCTF
348.	C2	NCTF
349.	A35	NCTF
350.	D35	NCTF
351.	C34	NCTF
352.	FH34	NCTF
353.	FE34	NCTF
354.	FG35	NCTF

7.2 Pin List for x8 (Package Side) Pinout

Table 7-2. Pin List for x8 (Package Side) Pinout

	Pin Number	Signal
1.	AM1	GND
2.	AF1	GND
3.	V1	GND
4.	M1	GND
5.	F1	GND
6.	AU2	GND
7.	AR2	GND
8.	AJ2	GND
9.	AC2	GND
10.	R2	GND
11.	J2	GND

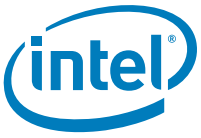

Table 7-2. Pin List for x8 (Package Side) Pinout

	Pin Number	Signal
12.	C2	GND
13.	A2	GND
14.	AM3	GND
15.	AH3	GND
16.	AF3	GND
17.	AB3	GND
18.	Y3	GND
19.	V3	GND
20.	T3	GND
21.	M3	GND
22.	K3	GND
23.	F3	GND
24.	AR4	GND
25.	AN4	GND
26.	AJ4	GND
27.	AA4	GND
28.	U4	GND
29.	J4	GND
30.	E4	GND
31.	C4	GND
32.	AT5	GND
33.	AP5	GND
34.	AM5	GND
35.	AK5	GND
36.	AH5	GND
37.	AF5	GND
38.	AD5	GND
39.	AB5	GND
40.	T5	GND
41.	P5	GND
42.	M5	GND
43.	K5	GND
44.	H5	GND
45.	F5	GND
46.	D5	GND
47.	B5	GND
48.	AL6	GND
49.	W6	GND
50.	G6	GND
51.	AH7	GND
52.	AF7	GND
53.	Y7	GND

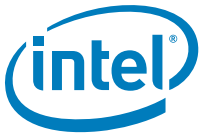

Table 7-2. Pin List for x8 (Package Side) Pinout

	Pin Number	Signal
54.	V7	GND
55.	M7	GND
56.	K7	GND
57.	AU8	GND
58.	AR8	GND
59.	AN8	GND
60.	AJ8	GND
61.	AE8	GND
62.	AA8	GND
63.	U8	GND
64.	N8	GND
65.	J8	GND
66.	E8	GND
67.	C8	GND
68.	A8	GND
69.	AP9	GND
70.	AH9	GND
71.	AF9	GND
72.	Y9	GND
73.	V9	GND
74.	M9	GND
75.	K9	GND
76.	D9	GND
77.	AR10	GND
78.	C10	GND
79.	AT11	GND
80.	AM11	GND
81.	AK11	GND
82.	AD11	GND
83.	AB11	GND
84.	T11	GND
85.	P11	GND
86.	H11	GND
87.	F11	GND
88.	AN12	GND
89.	E12	GND
90.	AM13	GND
91.	AK13	GND
92.	AD13	GND
93.	AB13	GND
94.	T13	GND
95.	P13	GND

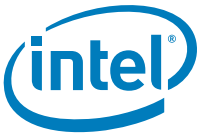

Table 7-2. Pin List for x8 (Package Side) Pinout

	Pin Number	Signal
96.	H13	GND
97.	F13	GND
98.	B13	GND
99.	AR14	GND
100.	C14	GND
101.	AP15	GND
102.	AH15	GND
103.	AF15	GND
104.	Y15	GND
105.	V15	GND
106.	M15	GND
107.	K15	GND
108.	D15	GND
109.	AU16	GND
110.	AR16	GND
111.	AN16	GND
112.	AJ16	GND
113.	AE16	GND
114.	AA16	GND
115.	U16	GND
116.	N16	GND
117.	J16	GND
118.	C16	GND
119.	A16	GND
120.	AH17	GND
121.	AF17	GND
122.	Y17	GND
123.	V17	GND
124.	M17	GND
125.	K17	GND
126.	AL18	GND
127.	W18	GND
128.	G18	GND
129.	AT19	GND
130.	AP19	GND
131.	AM19	GND
132.	AK19	GND
133.	AH19	GND
134.	AF19	GND
135.	AD19	GND
136.	AB19	GND
137.	T19	GND

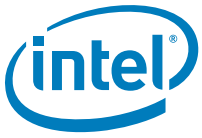

Table 7-2. Pin List for x8 (Package Side) Pinout

	Pin Number	Signal
138.	P19	GND
139.	M19	GND
140.	K19	GND
141.	H19	GND
142.	F19	GND
143.	D19	GND
144.	B19	GND
145.	AR20	GND
146.	AN20	GND
147.	AJ20	GND
148.	AA20	GND
149.	U20	GND
150.	J20	GND
151.	E20	GND
152.	C20	GND
153.	AM21	GND
154.	AH21	GND
155.	AF21	GND
156.	AB21	GND
157.	Y21	GND
158.	V21	GND
159.	T21	GND
160.	M21	GND
161.	K21	GND
162.	F21	GND
163.	AU22	GND
164.	AR22	GND
165.	AJ22	GND
166.	AC22	GND
167.	R22	GND
168.	J22	GND
169.	C22	GND
170.	A22	GND
171.	AM23	GND
172.	AF23	GND
173.	Y23	GND
174.	M23	GND
175.	F23	GND
176.	AG10	VD_PWR
177.	L10	VD_PWR
178.	AH11	VD_PWR
179.	AF11	VD_PWR

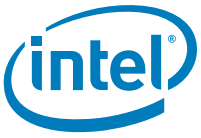

Table 7-2. Pin List for x8 (Package Side) Pinout

	Pin Number	Signal
180.	M11	VD_PWR
181.	K11	VD_PWR
182.	AJ12	VD_PWR
183.	AE12	VD_PWR
184.	N12	VD_PWR
185.	J12	VD_PWR
186.	AH13	VD_PWR
187.	AF13	VD_PWR
188.	M13	VD_PWR
189.	K13	VD_PWR
190.	AG14	VD_PWR
191.	L14	VD_PWR
192.	AM7	VD_PWR
193.	AK7	VD_PWR
194.	AD7	VD_PWR
195.	AB7	VD_PWR
196.	T7	VD_PWR
197.	P7	VD_PWR
198.	H7	VD_PWR
199.	F7	VD_PWR
200.	AM9	VD_PWR
201.	AK9	VD_PWR
202.	AD9	VD_PWR
203.	AB9	VD_PWR
204.	T9	VD_PWR
205.	P9	VD_PWR
206.	H9	VD_PWR
207.	F9	VD_PWR
208.	AL10	VD_PWR
209.	AC10	VD_PWR
210.	W10	VD_PWR
211.	R10	VD_PWR
212.	G10	VD_PWR
213.	Y11	VD_PWR
214.	V11	VD_PWR
215.	AA12	VD_PWR
216.	U12	VD_PWR
217.	Y13	VD_PWR
218.	V13	VD_PWR
219.	AL14	VD_PWR
220.	AC14	VD_PWR
221.	W14	VD_PWR

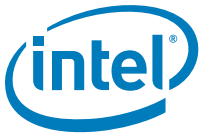

Table 7-2. Pin List for x8 (Package Side) Pinout

	Pin Number	Signal
222.	R14	VD_PWR
223.	G14	VD_PWR
224.	AM15	VD_PWR
225.	AK15	VD_PWR
226.	AD15	VD_PWR
227.	AB15	VD_PWR
228.	T15	VD_PWR
229.	P15	VD_PWR
230.	H15	VD_PWR
231.	F15	VD_PWR
232.	AM17	VD_PWR
233.	AK17	VD_PWR
234.	AD17	VD_PWR
235.	AB17	VD_PWR
236.	T17	VD_PWR
237.	P17	VD_PWR
238.	H17	VD_PWR
239.	F17	VD_PWR
240.	B9	A_PETp0
241.	A10	A_PETn0
242.	C6	A_PETp1
243.	D7	A_PETn1
244.	B3	A_PETp2
245.	A4	A_PETn2
246.	E2	A_PETp3
247.	D1	A_PETn3
248.	AB1	A_PETp4
249.	AA2	A_PETn4
250.	AE4	A_PETp5
251.	AD3	A_PETn5
252.	AH1	A_PETp6
253.	AG2	A_PETn6
254.	AL4	A_PETp7
255.	AK3	A_PETn7
256.	B15	A_PERp0
257.	A14	A_PERn0
258.	C18	A_PERp1
259.	D17	A_PERn1
260.	B21	A_PERp2
261.	A20	A_PERn2
262.	E22	A_PERp3
263.	D23	A_PERn3

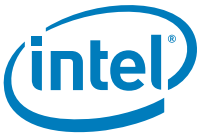

Table 7-2. Pin List for x8 (Package Side) Pinout

	Pin Number	Signal
264.	AB23	A_PERp4
265.	AA22	A_PERn4
266.	AE20	A_PERp5
267.	AD21	A_PERn5
268.	AH23	A_PERp6
269.	AG22	A_PERn6
270.	AL20	A_PERp7
271.	AK21	A_PERn7
272.	H21	B_PETp0
273.	G20	B_PETn0
274.	L22	B_PETp1
275.	K23	B_PETn1
276.	P21	B_PETp2
277.	N20	B_PETn2
278.	U22	B_PETp3
279.	T23	B_PETn3
280.	AP23	B_PETp4
281.	AN22	B_PETn4
282.	AU20	B_PETp5
283.	AT21	B_PETn5
284.	AP17	B_PETp6
285.	AR18	B_PETn6
286.	AU14	B_PETp7
287.	AT15	B_PETn7
288.	H3	B_PERp0
289.	G4	B_PERn0
290.	L2	B_PERp1
291.	K1	B_PERn1
292.	P3	B_PERp2
293.	N4	B_PERn2
294.	U2	B_PERp3
295.	T1	B_PERn3
296.	AP1	B_PERp4
297.	AN2	B_PERn4
298.	AU4	B_PERp5
299.	AT3	B_PERn5
300.	AP7	B_PERp6
301.	AR6	B_PERn6
302.	AU10	B_PERp7
303.	AT9	B_PERn7
304.	Y5	REFCLK+
305.	V5	REFCLK-

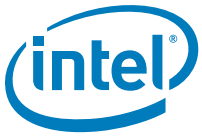

Table 7-2. Pin List for x8 (Package Side) Pinout

	Pin Number	Signal
306.	Y19	REFCLK_Out+
307.	V19	REFCLK_Out-
308.	Y1	PERST#
309.	B11	CLKREQ#
310.	AC18	JTAG_TDI
311.	L18	JTAG_TDO
312.	E16	JTAG_TMS
313.	AG18	JTAG_TCK
314.	R18	JTAG_TRST#
315.	AC6	SMBCLK
316.	AG6	SMBDAT
317.	R6	SMB_ADDR_1
318.	L6	SMB_ADDR_2
319.	V23	SMB_ADDR_3/VD_12
320.	AP11	EE_CLK/VD_5
321.	AP13	EE_DAT/VD_6
322.	AT1	VD_1
323.	W2	VD_2
324.	B1	VD_3
325.	AU12	VD_4
326.	D11	VD_7
327.	D13	VD_8
328.	A12	VD_9
329.	W22	VD_10
330.	AT23	VD_11
331.	B23	VD_13
332.	AT13	RX_DET_BYP

7.3 Pin List for x4 (Package Side) Pinout

Table 7-3. Pin List for x4 (Package Side) Pinout

	Pin Number	Signal
1.	T1	GND
2.	N1	GND
3.	K1	GND
4.	G1	GND
5.	D1	GND
6.	U2	GND
7.	R2	GND
8.	P2	GND
9.	M2	GND

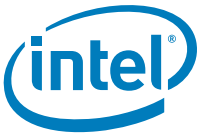

Table 7-3. Pin List for x4 (Package Side) Pinout

	Pin Number	Signal
10.	L2	GND
11.	J2	GND
12.	H2	GND
13.	F2	GND
14.	E2	GND
15.	C2	GND
16.	V3	GND
17.	B3	GND
18.	V4	GND
19.	B4	GND
20.	V5	GND
21.	R5	GND
22.	N5	GND
23.	L5	GND
24.	J5	GND
25.	G5	GND
26.	E5	GND
27.	B5	GND
28.	V6	GND
29.	R6	GND
30.	N6	GND
31.	L6	GND
32.	J6	GND
33.	G6	GND
34.	E6	GND
35.	B6	GND
36.	V7	GND
37.	B7	GND
38.	V8	GND
39.	B8	GND
40.	U9	GND
41.	R9	GND
42.	P9	GND
43.	M9	GND
44.	L9	GND
45.	J9	GND
46.	H9	GND
47.	F9	GND
48.	E9	GND
49.	C9	GND
50.	T10	GND
51.	N10	GND

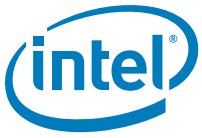

Table 7-3. Pin List for x4 (Package Side) Pinout

	Pin Number	Signal
52.	K10	GND
53.	G10	GND
54.	D10	GND
55.	K7	VD_PWR
56.	M8	VD_PWR
57.	L8	VD_PWR
58.	J8	VD_PWR
59.	H8	VD_PWR
60.	T3	VD_PWR
61.	R3	VD_PWR
62.	P3	VD_PWR
63.	M3	VD_PWR
64.	L3	VD_PWR
65.	J3	VD_PWR
66.	H3	VD_PWR
67.	F3	VD_PWR
68.	E3	VD_PWR
69.	D3	VD_PWR
70.	T4	VD_PWR
71.	P4	VD_PWR
72.	M4	VD_PWR
73.	K4	VD_PWR
74.	H4	VD_PWR
75.	F4	VD_PWR
76.	D4	VD_PWR
77.	T7	VD_PWR
78.	P7	VD_PWR
79.	M7	VD_PWR
80.	H7	VD_PWR
81.	F7	VD_PWR
82.	D7	VD_PWR
83.	T8	VD_PWR
84.	R8	VD_PWR
85.	P8	VD_PWR
86.	F8	VD_PWR
87.	E8	VD_PWR
88.	D8	VD_PWR
89.	A3	A_PETp0
90.	A4	A_PETn0
91.	C1	A_PETp1
92.	B1	A_PETn1
93.	F1	A_PETp2

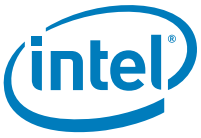

Table 7-3. Pin List for x4 (Package Side) Pinout

	Pin Number	Signal
94.	E1	A_PETn2
95.	J1	A_PETp3
96.	H1	A_PETn3
97.	A8	A_PERp0
98.	A7	A_PERn0
99.	C10	A_PERp1
100.	B10	A_PERn1
101.	F10	A_PERp2
102.	E10	A_PERn2
103.	J10	A_PERp3
104.	H10	A_PERn3
105.	M10	B_PETp0
106.	L10	B_PETn0
107.	R10	B_PETp1
108.	P10	B_PETn1
109.	V10	B_PETp2
110.	U10	B_PETn2
111.	W7	B_PETp3
112.	W8	B_PETn3
113.	M1	B_PERp0
114.	L1	B_PERn0
115.	R1	B_PERp1
116.	P1	B_PERn1
117.	V1	B_PERp2
118.	U1	B_PERn2
119.	W4	B_PERp3
120.	W3	B_PERn3
121.	C5	REFCLK+
122.	C6	REFCLK-
123.	U5	REFCLK_Out+
124.	U6	REFCLK_Out-
125.	A2	PERST#
126.	A9	CLKREQ#
127.	U3	JTAG_TDI
128.	C3	JTAG_TDO
129.	N3	JTAG_TMS
130.	K3	JTAG_TCK
131.	G3	JTAG_TRST#
132.	G8	SMBCLK
133.	K8	SMBDAT
134.	W5	SMB_ADDR_1
135.	W6	SMB_ADDR_2

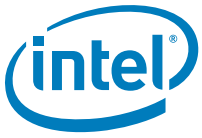

Table 7-3. Pin List for x4 (Package Side) Pinout

	Pin Number	Signal
136.	W9	SMB_ADDR_3/VD_10
137.	U8	EE_DAT/VD_7
138.	N8	EE_CLK/VD_8
139.	W1	VD_1
140.	W2	VD_2
141.	W10	VD_3
142.	A1	VD_4
143.	A5	VD_5
144.	A10	VD_6
145.	C8	VD_9
146.	A6	RX_DET_BYP

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