



# Intel® Agilex™ FPGAs and SoCs Advanced Information Brief

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(Device Overview)



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## 1. Intel® Agilinx™ FPGA and SoC Device Overview

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Intel's 10-nm Intel® Agilinx™ FPGAs and SoCs are built using an innovative chiplet architecture, which provides agile and flexible integration of heterogeneous technology elements in a System-in-Package (SiP). The chiplet architecture enables Intel to address a broad array of acceleration and high-bandwidth applications with tailored and flexible solutions. Leveraging advanced 3D packaging technology such as Intel Embedded Multi-Die Interconnect Bridge (EMIB), the chiplet approach allows the combination of traditional FPGA die with purpose-built semiconductor die to create devices that are uniquely optimized for target applications.

Delivering up to 40% higher core performance, or up to 40% lower power over previous generation high-performance FPGAs, Intel Agilinx FPGAs and SoCs accelerate system engineers' delivery of today's and tomorrow's most advanced high-bandwidth applications through groundbreaking features:

- Advanced analog functions such as 116 Gbps PAM-4 transceivers
- High-bandwidth processor interface interconnect including PCIe\* Gen5 and industry's first Compute Express Link (CXL) in an FPGA
- Up to 4 x 400GE or 8 x 200GE network interface connectivity in one device
- Fourth generation scalable integrated memory controllers including support for DDR5, and Intel Optane™ persistent memory technology
- Industry leading DSP support with up to 40 TFLOPs
- Second generation Intel Hyperflex™ core fabric

With Intel One API Software, software developers can use Intel Agilinx FPGAs and SoCs as an acceleration solution. The Intel One API Software provides a unified, single-source, software-friendly heterogeneous programming environment for diverse computing engines. The software includes a comprehensive and unified portfolio of developer tools for mapping software to the hardware that can accelerate the code.

*Note:* The information contained in this document is preliminary and subject to change.

### Key Innovations in Intel Agilinx FPGAs and SoCs

- Intel Advanced 10nm FinFET (3rd generation) process
- Innovative chiplet architecture allowing agile and flexible integration of heterogeneous technologies in a System-in-Package (SiP) for highly specific application requirements
- Second Generation Intel Hyperflex core fabric delivering up to 40% higher performance than previous generation high-performance FPGAs
- Device densities of over 3 million equivalent logic elements (LEs)
- Transceiver data rates up to 116 Gbps



- Configurable networking support including Hard 10/25/50/100/200/400 GE MAC, PCS, FEC in select tiles with IEEE 1588 support
- Up to 4 x 400GE or 8 x 200GE networking capability in one device
- Hard PCI Express\* Gen4 x16 (up to 16 Gbps per lane) and Gen5 x16 (up to 32 Gbps per lane) intellectual property (IP) blocks with port bifurcation support for 2x8 endpoint or 4x4 rootport
- Compute Express Link (CXL) Hard IP block for cache-coherent and memory-coherent interfacing to Intel Xeon® Scalable Processors
- Hard memory controllers and PHY supporting DDR4 x72 at 3200 Mbps per pin, DDR5 x72 at 4400 Mbps per pin and Intel Optane persistent memory support
- Device options supporting up to 16 GB of high bandwidth memory
- Hard fixed-point and IEEE 754 compliant hard floating-point variable precision digital signal processing (DSP) blocks providing up to 40 TFLOPS of FP16 or BFLOAT16 compute performance
- Over 17K of 18x19 multipliers, or over 34K of 9x9 multipliers in a single device
- Multi-level on-chip memory hierarchy with over 300 Mb of embedded RAM in the largest device, made up of 640b MLABs, 20 Kb M20K blocks, and 18 Mb eSRAM memory blocks
- Quad-core 64-bit Arm\* Cortex\* A53 embedded processors running up to 1.4 GHz in SoC family variants
- Programmable clock tree synthesis for flexible, low power, low skew clocking
- Fractional synthesis and ultra-low jitter LC tank based transmit phase locked loops (PLLs)
- Rectangular Packaging and Hex Pattern Ball Array to support more functionality / area while simplifying BOM list
- Dedicated Secure Device Manager (SDM) that:
  - Manages Boot Process, Encryption, Authentication, and all Keys
  - Manages Tamper Sensors, and Scripted Device Erasure
  - Provides Secure Boot Support for Private Key Root Trust on FPGA, Public Key only on FPGA, and Physically Unclonable Function (PUF)-Based Keys
  - Provides Platform Attestation
- Comprehensive set of advanced power saving features that deliver up to 40% lower power compared to previous generation high-performance FPGAs
- Non-destructive register state readback and writeback, to support ASIC prototyping and other applications



## 1.1. Intel Agilex FPGA and SoC Family Variants

### 1.1.1. Intel Agilex F-Series SoC FPGAs

Intel Agilex F-Series SoC FPGAs are optimized for a wide range of applications that require optimal balance of power and performance, with the power efficiency of Intel's industry-leading 10-nm FinFET process technology. These devices deliver up to 40% increase in core fabric performance compared to the previous generation of Intel FPGAs and contain up to 2.7 million LEs and 289 Mb of on-chip RAM. They also feature general purpose transceivers, PCIe Gen4 x16, and 3200 Mbps DDR4 external memory interface performance. The transceivers are capable of up to 32 Gbps (NRZ) and 58 Gbps (PAM4). The SoC devices contains an embedded quad-core 64-bit Arm Cortex-A53 hard processor system.

### 1.1.2. Intel Agilex I-Series SoC FPGAs

Intel Agilex I-Series SoC FPGAs offer high-performance processor interfaces and transceiver rates for bandwidth-intensive applications. The Intel Agilex I-Series SoC FPGAs contain transceivers that are capable of up to 116 Gbps (PAM4) and configurable networking support up to 4 x 400G in a single device, including hard Ethernet MAC, PCS, FEC for up to 400GE. They also feature PCIe Gen5 x16 with data rate of 32 Gbps, and industry's first Compute Express Link (CXL) implementation in an FPGA. The Intel Agilex I-Series include an embedded quad-core 64-bit Arm Cortex-A53 hard processor system.

### 1.1.3. Intel Agilex M-Series SoC FPGAs

Intel Agilex M-Series SoC FPGAs offer processor and memory interfaces for compute-intensive, high-memory bandwidth applications. The Intel Agilex M-Series SoC FPGAs contain over 3 million LEs, over 300 Mb of on-chip RAM, and DSP support up to 40 TFLOPs. It also includes PCIe Gen5 x16 with data rate of 32 Gbps, Compute Express Link (CXL), HBM option, Intel Optane Persistent Memory support, and 4400 Mbps DDR5 external memory interface performance. The Intel Agilex M-Series SoC FPGAs include an embedded quad-core 64-bit Arm Cortex-A53 hard processor system.

### 1.1.4. Common Features

Common to all Intel Agilex FPGAs family variants is a high-performance fabric based on the second generation Intel Hyperflex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

- On-chip multi-level memory hierarchy blocks including MLAB (640 b), M20K (20 Kb), and eSRAM (18 Mb)
- Variable precision DSP blocks with hard IEEE 754 compliant floating-point units, including support for single-precision FP32 (32-bit arithmetic), half-precision FP16 (16-bit arithmetic) floating point modes and BFLOAT16 floating-point format.
- Integer PLLs
- Hard memory controllers and PHY for external memory interfaces
- General purpose I/O cells



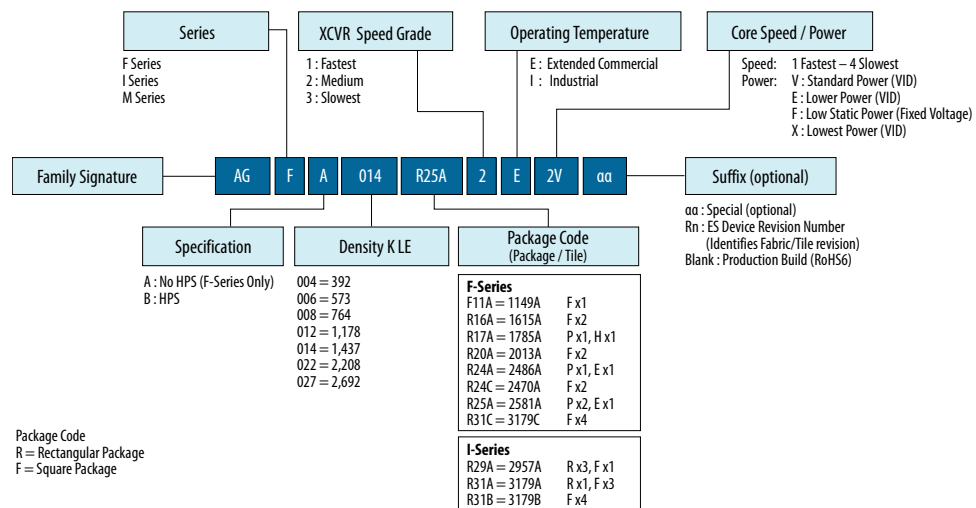
To clock these building blocks, Intel Agilex FPGA devices employ programmable clock tree synthesis using a dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while under operation.

All family variants' high speed serial transceivers contain both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols such as 10/25/100 GE MAC, PCS, FEC in E-tiles, and 10/25/50/100/200/400 GE MAC, PCS, FEC in F-tiles.

In addition to the hard PCS, Intel Agilex FPGAs devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3/Gen4/Gen5 rates in x1/x2/x4/x8/x16 lane configurations (Gen5 in Intel Agilex I-series and M-series devices). The hard PCS, and PCI Express IP free up valuable core logic resources, save power and increase your productivity.

## 1.2. Available Options

Figure 1. Intel Agilex Ordering Part Number (OPN)

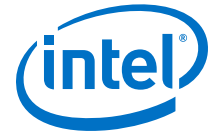


## 1.3. Intel Agilex FPGA and SoC Summary of Features

Table 1. Feature Summary

Feature	Description
<b>Technology</b>	<ul style="list-style-type: none"> <li>10-nm Intel Tri-Gate (FinFET) process technology</li> <li>SmartVID controlled core voltage, standard power devices</li> <li>0.8-V fixed core voltage, low static power devices</li> </ul>
<b>Low power serial Transceivers</b>	<p><b>PCIe (P-Tile and F-Tile)</b></p> <ul style="list-style-type: none"> <li>— PCIe rates up to Gen4, 16 Gbps in NRZ mode</li> </ul> <p><b>PCIe (R-Tile)</b></p> <ul style="list-style-type: none"> <li>PCIe rates up to Gen5, 32 Gbps in NRZ mode</li> <li>Compute Express Link (CXL) support</li> </ul> <p><b>PCIe (H-Tile)</b></p>

*continued...*



Feature	Description
	<ul style="list-style-type: none"> <li>• PCIe Gen3 x8 in NRZ mode</li> </ul> <p><b>Networking (E-Tile)</b></p> <ul style="list-style-type: none"> <li>• Continuous operating range of 1 Gbps to 28.9 Gbps in NRZ mode and 2 Gbps to 58 Gbps in PAM4 mode</li> <li>• Insertion loss compliant to 802.3bj, CEI 25G-LR, and CEI 56G-LR</li> <li>• Oversampling capability for data rates below 1 Gbps</li> <li>• ATX transmit PLLs (LC-PLL) with user-configurable fractional synthesis capability</li> <li>• XFP, QSFP-DD, OSFP, QSFP/QSFP28, QSFP56, SFP+, SFP28, SFP56, CFP/CFP2/CFP4 optical module support</li> <li>• Adaptive linear and decision feedback equalization</li> <li>• Transmit pre-emphasis and de-emphasis</li> <li>• Dynamic partial reconfiguration of individual transceiver channels</li> <li>• On-chip instrumentation (Eye Viewer non-intrusive data eye monitoring)</li> </ul> <p><b>Networking (F-Tile)</b></p> <ul style="list-style-type: none"> <li>• Continuous operating range of 1 Gbps to 32 Gbps in NRZ mode and 20 Gbps to 58 Gbps in PAM4 mode</li> <li>• Operating ranges of 24-29 Gbps &amp; 48-58 Gbps in NRZ mode and 24-29 Gbps, 48-58 Gbps, &amp; 96-116 Gbps in PAM4 mode</li> </ul>
<b>General purpose I/Os</b>	<ul style="list-style-type: none"> <li>• Over 700 total GPIO available</li> <li>• 1.6 Gbps 1.5V True Differential Signaling compatible with LVDS/ RSDS/ Mini-LVDS/ LVPECL</li> <li>• 1600 MHz/3200 Mbps DDR4 external memory interface</li> <li>• 2200 MHz/4400 Mbps DDR5 external memory interface</li> <li>• 1.2 V single-ended LVCMOS interfacing</li> <li>• On-chip termination (OCT)</li> </ul>
<b>Embedded hard IP</b>	<ul style="list-style-type: none"> <li>• DDR4/DDR5/Intel Optane persistent memory hard memory controller (</li> <li>• RLD RAM3/QDR IV using soft memory controller</li> <li>• Multiple hard IP instantiations in each device</li> </ul>
<b>Transceiver hard IP</b>	<p><b>PCIe (P-Tile and F-Tile)</b></p> <ul style="list-style-type: none"> <li>• Up to Gen4 x 16 EP and RP</li> <li>• Port Bifurcation support: 2 x 8 Endpoint or 4 x 4 Rootport</li> <li>• TL Bypass Feature</li> <li>• SR-IOV (8 physical functions / 2K virtual functions)</li> <li>• VirtIO support</li> <li>• Scalable IOV</li> <li>• Shared Virtual Memory</li> </ul> <p><b>PCIe (R-Tile)</b></p> <ul style="list-style-type: none"> <li>• Up to Gen5 x 16 EP and RP</li> <li>• Port Bifurcation support: 2 x 8 Endpoint or 4 x 4 Rootport</li> <li>• TL Bypass Feature</li> <li>• SR-IOV (8 physical functions / 2K virtual functions)</li> <li>• VirtIO support</li> <li>• Scalable IOV</li> <li>• Shared Virtual Memory</li> <li>• PIPE Direct mode</li> <li>• Precise Time Management</li> </ul> <p><b>Networking (E-Tile)</b></p> <ul style="list-style-type: none"> <li>• Ethernet IP Configurations           <ul style="list-style-type: none"> <li>— 24 x 10/25GE MAC, PCS, RS-FEC</li> <li>— 4 x 100GE MAC, PCS, RS-FEC</li> </ul> </li> <li>• CPRI and Fibre Channel FECs</li> <li>• CR/KR (AN/LT)</li> </ul>

*continued...*



Feature	Description
	<ul style="list-style-type: none"> <li>• 1588 PTP</li> <li>• MAC, PCS, and FEC bypass options</li> <li>• PMA Direct Mode</li> </ul> <p><b>Networking (F-Tile)</b></p> <ul style="list-style-type: none"> <li>• Ethernet IP Configurations:               <ul style="list-style-type: none"> <li>– 16 x 10/25GE MAC, PCS, FEC</li> <li>– 8 x 50GE MAC, PCS, FEC</li> <li>– 4 x 100GE MAC, PCS, FEC</li> <li>–</li> <li>– 1 x 400GE MAC, PCS, FEC</li> </ul> </li> <li>• KP FEC support for up to 600G Interlaken</li> <li>• Flex-O FEC, FlexE PCS and FEC, Ethernet over OTN Mode, SyncE, Fibre Channel, CPRI FEC</li> <li>• CR/KR (AN/LT)</li> <li>• 1588 PTP</li> <li>• MAC, PCS, and FEC bypass options</li> <li>• PMA Direct Mode</li> </ul> <p><b>H-Tile</b></p> <ul style="list-style-type: none"> <li>• 1x PCIe Gen3 x8(1) (with SR-IOV)</li> <li>• 4 Physical Functions, 2K Virtual Functions</li> <li>• Ethernet IP Configurations 1x 100 GbE MAC or 50 GbE MAC</li> <li>• PMA Direct Mode</li> </ul>
<b>Power management</b>	<ul style="list-style-type: none"> <li>• SmartVID controlled core voltage, standard power devices</li> <li>• Fixed core voltage and low static power devices available</li> <li>• Intel Quartus® Prime Pro Edition integrated power analysis</li> </ul>
<b>High performance core fabric</b>	<ul style="list-style-type: none"> <li>• Second Generation Intel Hyperflex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks</li> <li>• Enhanced adaptive logic module (ALM)</li> <li>• Improved multi-track routing architecture reduces congestion and improves compile times</li> <li>• Hierarchical core clocking architecture with programmable clock tree synthesis</li> <li>• Fine-grained partial reconfiguration</li> </ul>
<b>Internal memory blocks</b>	<ul style="list-style-type: none"> <li>• M20K: 20 Kbit with hard ECC support</li> <li>• MLAB: 640-bit distributed LUTRAM</li> <li>• eSRAM: 18 Mb embedded memory block with hard ECC support</li> </ul>
<b>Variable precision DSP blocks</b>	<ul style="list-style-type: none"> <li>• IEEE 754-compliant hard single-precision floating point capability</li> <li>• Supports Half Precision FP16 and BFLOAT16</li> <li>• Supports signal processing with precision ranging from 9x9 up to 54x54</li> <li>• Native 27x27, 18x19, and 9x9 multiply modes</li> <li>• 64-bit accumulator and cascade for systolic 200GE FIRs</li> <li>• Internal coefficient memory banks</li> <li>• Pre-adder/subtractor improves efficiency</li> <li>• 2 xAdditional pipeline register increases performance and reduces power</li> </ul>
<b>Phase locked loops (PLL)</b>	<ul style="list-style-type: none"> <li>• Precision frequency synthesis</li> <li>• Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS Compatible Interfaces, clock delay compensation, zero delay buffering</li> </ul>
<i>continued...</i>	





Feature	Description
<b>Core clock networks</b>	<ul style="list-style-type: none"> <li>800 MHz external memory interface clocking, supports 3200 Mbps DDR4 interface</li> <li>800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface through 1.5 V True Differential Signaling compatible with LVDS/ RSDS/ Mini-LVDS/ LVPECL</li> <li>Programmable clock tree synthesis, backwards compatible with global, regional and peripheral clock networks</li> <li>Clocks only synthesized where needed, to minimize dynamic power</li> </ul>
<b>Configuration</b>	<ul style="list-style-type: none"> <li>Dedicated Secure Device Manager</li> <li>Software programmable device configuration</li> <li>Serial and parallel flash interface</li> <li>Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3/Gen4/ Gen5</li> <li>Fine-grained partial reconfiguration of core fabric</li> <li>Dynamic reconfiguration of transceivers and PLLs</li> <li>Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators, and multi-factor authentication</li> <li>Physically Unclonable Function (PUF) service</li> <li>Platform Attestation</li> <li>Anti Tamper Feature</li> </ul>
<b>Packaging</b>	<ul style="list-style-type: none"> <li>Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology</li> <li>Multiple devices with identical package footprints allows seamless migration across different device densities</li> <li>Mixture of ball pitch FBGA packages, 1 mm, 0.92 mm, 0.8 mm and several mixed pitch packages</li> <li>Rectangular Package and Hexagonal Ball Grid (Mixture of grid &amp; Hex patterns)</li> </ul>
<b>Software and Tools</b>	<ul style="list-style-type: none"> <li>Intel Quartus Prime Pro Edition design suite with new compiler and Hyper-Aware design flow</li> <li>Fast Forward compiler to allow Intel Hyperflex architecture performance exploration</li> <li>Transceiver toolkit</li> <li>Platform Designer integration tool</li> <li>DSP Builder advanced blockset</li> <li>OpenCL* support</li> <li>SoC Embedded Design Suite (EDS)</li> </ul>

**Table 2. Intel Agilix SoC Specific Device Features**

SoC Subsystem	Feature	Description
<b>Hard Processor System</b>	Multi-processor unit (MPU) core	<ul style="list-style-type: none"> <li>Quad-core Arm Cortex-A53 MPCore processor with Arm CoreSight™ debug and trace technology</li> <li>Scalar floating-point unit supporting single and double precision</li> <li>Arm NEON™ media processing engine for each processor</li> </ul>
	System Controllers	<ul style="list-style-type: none"> <li>System Memory Management Unit (SMMU)</li> <li>Cache Coherency Unit (CCU)</li> </ul>
	Layer 1 Cache	<ul style="list-style-type: none"> <li>32 KB L1 instruction cache with parity</li> <li>32 KB L1 data cache with ECC</li> </ul>
	Layer 2 Cache	<ul style="list-style-type: none"> <li>1 MB Shared L2 Cache with ECC</li> </ul>
	On-Chip Memory	<ul style="list-style-type: none"> <li>256 KB On-Chip RAM</li> </ul>
	Direct memory access (DMA) controller	<ul style="list-style-type: none"> <li>8-Channel DMA</li> </ul>

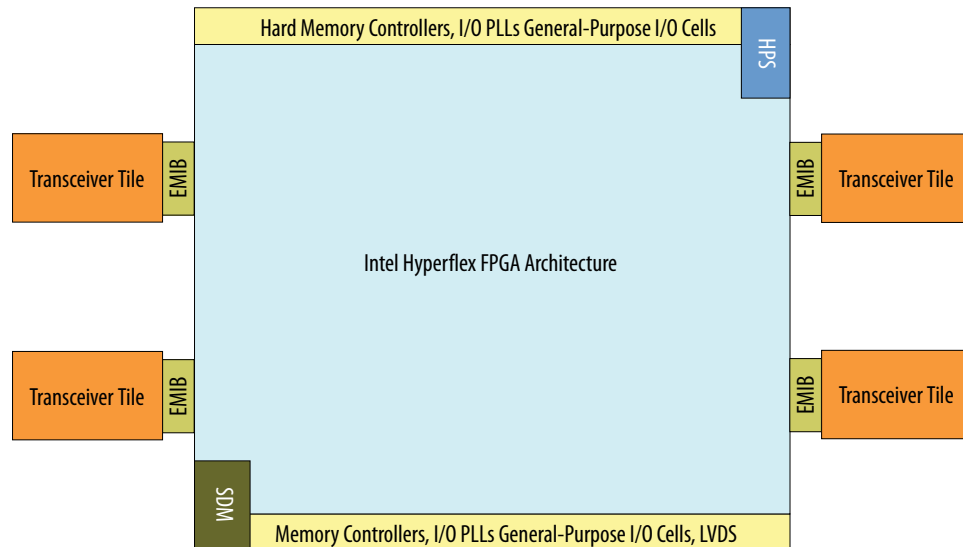
*continued...*



SoC Subsystem	Feature	Description
	Ethernet media access controller (EMAC)	<ul style="list-style-type: none"> <li>Three 10/100/1000 EMAC with integrated DMA</li> </ul>
	USB On-The-Go controller (OTG)	<ul style="list-style-type: none"> <li>2 USB OTG with integrated DMA</li> </ul>
	UART controller	<ul style="list-style-type: none"> <li>2 UART 16550 compatible</li> </ul>
	Serial Peripheral Interface (SPI) controller	<ul style="list-style-type: none"> <li>4 SPI</li> </ul>
	I <sup>2</sup> C controller	<ul style="list-style-type: none"> <li>5 I<sup>2</sup>C controllers</li> </ul>
	SD/SDIO/MMC controller	<ul style="list-style-type: none"> <li>1 eMMC version 4.5 with DMA and CE-ATA support</li> <li>SD, including eSD, version 3.0</li> <li>SDIO, including eSDIO, version 3.0</li> <li>CE-ATA - version 1.1</li> </ul>
	NAND flash controller	<ul style="list-style-type: none"> <li>1 ONFI 1.0, 8- and 16-bit support</li> </ul>
	General-purpose I/O (GPIO)	<ul style="list-style-type: none"> <li>Maximum of 48 software programmable GPIO</li> </ul>
	Timers	<ul style="list-style-type: none"> <li>4 general-purpose timers</li> <li>4 watchdog timers</li> </ul>
<b>Secure Device Manager</b>	Security	<ul style="list-style-type: none"> <li>Secure Boot</li> <li>Advanced Encryption Standard (AES) and authentication (SHA/ECDsa)</li> </ul>
<b>External Memory Interface</b>	External Memory Interface	<ul style="list-style-type: none"> <li>Hard Memory Controller with DDR4</li> </ul>

## 1.4. Intel Agilex FPGA and SoC Block Diagram

Figure 2. Intel Agilex FPGA Block Diagram





## 1.5. Intel Agilex FPGA and SoC Family Plan

**Table 3. Intel Agilex F-Series FPGAs and SoCs Family Plan Part-1**

Intel Agilex F-Series Device Names	Logic Elements (LE)	eSRAM Blocks	eSRAM Mbits	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	Variable Precision DSP Blocks	18x19 Multipliers
AGF 004	391,996	0	0	1,900	37	6,644	4	1,150	2300
AGF 006	573,480	0	0	2,844	56	9,720	6	1,640	3280
AGF 008	764,640	0	0	3,792	74	12,960	8	2,296	4592
AGF 012	1,178,525	2	36	5,900	115	19,975	12	3,743	7486
AGF 014	1,437,240	2	36	7,110	139	24,360	15	4,510	9020
AGF 022	2,208,075	0	0	10,900	212	37,425	23	6,250	12500
AGF 027	2,692,760	0	0	13,272	259	45,640	28	8,528	17056

**Table 4. Intel Agilex F-Series FPGAs and SoCs Family Plan Part-2**

Intel Agilex F-Series Device Names	F-Tile Transceiver Channels (1)	F-Tile Ethernet Blocks (2)	F-Tile PCIe Controllers (3)	P-Tile PCIe Controllers (4)	E-Tile Ethernet Blocks (5)	E-Tile Transceiver Channels (6)	H-Tile Transceiver Channels	HPS Option
AGF 004	24x PAM-4 32x NRZ	2	2	0	0	0	-	Yes
AGF 006	24x PAM-4 32x NRZ	2	2	0	0	0	-	Yes
AGF 008	24x PAM-4 32x NRZ	2	2	0	0	0	-	Yes
AGF 012	24x PAM-4 32x NRZ	2	2	1	4	8x PAM-4 16x NRZ	-	Yes

*continued...*

(1) Maximum F Tile Transceiver Channels PAM4 (up to 58 Gbps) - RS & KP FEC NRZ (up to 32 Gbps)

(2) Maximum F Tile 10/25/50/100/200/400G Ethernet MAC + FEC hard IP blocks

(3) Maximum F-Tile PCIe hard IP blocks (Gen4 x 16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP)

(4) Maximum P Tile PCIe hard IP blocks (Gen4x16 ) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP)

(5) Maximum E Tile 100G Ethernet MAC + FEC hard IP Blocks

(6) Maximum E Tile Transceiver Channels PAM4 (up to 58 Gbps) - RS & KP FEC NRZ (up to 28.9 Gbps)



Intel Agilex F-Series Device Names	F-Tile Transceiver Channels (1)	F-Tile Ethernet Blocks (2)	F-Tile PCIe Controllers (3)	P-Tile PCIe Controllers (4)	E-Tile Ethernet Blocks (5)	E-Tile Transceiver Channels (6)	H-Tile Transceiver Channels	HPS Option
AGF 014	24x PAM-4 32x NRZ	2	2	1	4	8x PAM-4 16x NRZ	16 x 28.3G NRZ or 24 x 17.4G NRZ	Yes
AGF 022	48x PAM-4 64x NRZ	4	4	2	4	12x PAM-4 24x NRZ	-	Yes
AGF 027	48x PAM-4 64x NRZ	4	4	2	4	12x PAM-4 24x NRZ	-	Yes

**Table 5. Intel Agilex F-Series FPGAs with F-Tile Package Options & I/O Pins**

*Note:* **Key:** GPIO (LVDS) / F-Tile 32G (58G) **Example:** If an entry in the table below contains 384(192)/32(24), it means 384 GPIO of which 192 are LVDS; thirty-two 32G NRZ channels or twenty-four 58G PAM4 channels

Intel Agilex F-Series Device Names	1149A (7)	1615A (8)	2013A (9)	2470A (10)	3179C (11)
AGF 004	360(180)/16(12)	384(192)/32(24)	384(192)/32(24)		
AGF 006	360(180)/16(12)	384(192)/32(24)	384(192)/32(24)		
AGF 008		384(192)/32(24)	576(288)/32(24)		
AGF 012			576(288)/32(24)	744(372)/32(24)	
<i>continued...</i>					

- (1) Maximum F Tile Transceiver Channels PAM4 (up to 58 Gbps) - RS & KP FEC NRZ (up to 32 Gbps)
- (2) Maximum F Tile 10/25/50/100/200/400G Ethernet MAC + FEC hard IP blocks
- (3) Maximum F-Tile PCIe hard IP blocks (Gen4 x 16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP)
- (4) Maximum P Tile PCIe hard IP blocks (Gen4x16 ) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP)
- (5) Maximum E Tile 100G Ethernet MAC + FEC hard IP Blocks
- (6) Maximum E Tile Transceiver Channels PAM4 (up to 58 Gbps) - RS & KP FEC NRZ (up to 28.9 Gbps)
- (7) (F-Tile x1) (29 mm x 29mm, Grid 0.8 pitch)
- (8) (F-Tile x2) (45 mm x 32 mm, Hex Mixed 1.0/0.92 mm pitch)
- (9) (F-Tile x2) (47 mm x 38mm, Hex Mixed 1.0/0.92mm pitch)
- (10) (F-Tile x2) (47 mm x 46mm, Hex Mixed 1.0/0.92mm pitch)
- (11) (F-Tile x4) (56 mm x 45 mm, Hex 0.92 mm)



Intel Agilex F-Series Device Names	1149A <sup>(7)</sup>	1615A <sup>(8)</sup>	2013A <sup>(9)</sup>	2470A <sup>(10)</sup>	3179C <sup>(11)</sup>
AGF 014			576(288)/32(24)	744(372)/32(24)	
AGF 022				744(372)/32(24)	720(360)/64(48)
AGF 027				744(372)/32(24)	720(360)/64(48)

**Table 6. Intel Agilex F-Series FPGAs with P-Tile and E-Tile Package Options & I/O Pins**

*Note:* **Key:** GPIO (LVDS) / E-Tile 28.9G (58G) / P-Tile 16G PCIe **Example:** If an entry in the table below contains 768(384)/16(8)/16, it means that 768 GPIO of which 384 are LVDS; sixteen 28.9 NRZ channels or eight 58G PAM4 channels; and sixteen up to 16G/lane PCIe

Intel Agilex F-Series Device Names	2486A <sup>(12)</sup>	2581A <sup>(13)</sup>
AGF 004		
AGF 006		
AGF 008		
AGF 012	768(384)/16(8)/16	624(312)/24(12)/16
AGF 014	768(384)/16(8)/16	624(312)/24(12)/16
AGF 022		624(312)/24(12)/32
AGF 027		624(312)/24(12)/32

**Table 7. Intel Agilex I-Series SoC FPGAs Family Plan Part-1**

Intel Agilex I-Series Device Names	Logic Elements (LE)	eSRAM Blocks	eSRAM Mbits	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	Variable Precision DSP Blocks	18x19 Multipliers
AGI 022	2,208,075	0	0	10,900	212	37,425	23	6,250	12.5K
AGI 027	2,692,760	0	0	13,272	259	45,640	28	8,528	17K

- (7) (F-Tile x1) (29 mm x 29mm, Grid 0.8 pitch)
- (8) (F-Tile x2) (45 mm x 32 mm, Hex Mixed 1.0/0.92 mm pitch)
- (9) (F-Tile x2) (47 mm x 38mm, Hex Mixed 1.0/0.92mm pitch)
- (10) (F-Tile x2) (47 mm x 46mm, Hex Mixed 1.0/0.92mm pitch)
- (11) (F-Tile x4) (56 mm x 45 mm, Hex 0.92 mm)
- (12) (E-Tile + P-Tile) (55 mm x 42.5 mm, Hex 1.0 mm pitch)
- (13) (E-Tile + P-Tile) (52.5 mm x 40.5 mm, Mixed 0.94/0.92 mm)



**Table 8. Intel Agilex I-Series SoC FPGAs Family Plan Part-2**

Intel Agilex I-Series Device Names	R-Tile PCIe blocks <sup>(14)</sup>	Compute Express Link (CXL) Lanes <sup>(15)</sup>	F-Tile Ethernet 400 GbE <sup>(16)</sup>	F-Tile PCIe <sup>(17)</sup>	F-Tile High Speed 116 Gbps <sup>(18)</sup>	F-Tile General Purpose 58 Gbps <sup>(19)</sup>	HPS
AGI 022	3	48	2 (Max 4 F-Tiles in the 3179B package)	3 (Maximum of four PCIe controllers in 3179B package)	8x PAM-4 8x NRZ	48x PAM-4 64x NRZ	Yes
AGI 027	3	48	2 (Max 4 F-Tiles in the 3179B package)	3 (Maximum of four PCIe controllers in 3179B package)	8x PAM-4 8x NRZ	48x PAM-4 64x NRZ	Yes

**Table 9. Intel Agilex I-Series FPGAs with F-Tile Package Options & I/O Pins**

*Note:* **Key:** GPIO (LVDS) / F-Tile 32G (58G) / High Speed 56G (116G). **Example:** If an entry in the table below contains 720(360)/64(48)/8(8), it means, 720 GPIO of which 360 are LVDS; sixty-four 32G NRZ channels and forty-eight 58G PAM4 channels; eight 56G NRZ channels and eight 116G PAM4 channels

Intel Agilex I-Series Device Names	3179B <sup>(20)</sup>
AGI 022	720(360)/64(48)/ 8(8)
AGI 027	720(360)/64(48)/ 8(8)

<sup>(14)</sup> Maximum R-Tile PCIe hard IP blocks (Gen5x16) or Bifurcateable 2x PCIe Gen5 x8 (EP) or 4x Gen5 x4 (RP)

<sup>(15)</sup> Maximum Compute Express Link (CXL) lanes for Intel Xeon Scalable Processor

<sup>(16)</sup> Maximum F Tile 10/25/50/100/200/400G Ethernet MAC + FEC hard IP blocks

<sup>(17)</sup> Maximum F- Tile PCIe hard IP blocks (Gen4x16 ) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP)

<sup>(18)</sup> Maximum F Tile High Speed Transceiver Channels blocks PAM4 (up to 116 Gbps) - RS & KP FEC NRZ (up to 58 Gbps)

<sup>(19)</sup> Maximum F Tile General Purpose Transceiver Channels PAM4 (up to 58 Gbps) - RS & KP FEC NRZ (up to 32 Gbps)

<sup>(20)</sup> (F-Tile x4) (56 mm x 45 mm, Hex 0.92 mm pitch)



**Table 10. Intel Agilex I-Series FPGAs with F-Tile and R-Tile Package Options & I/O Pins**

Note: **Key:** GPIO (LVDS) / F-Tile 32G (58G) / High Speed 58G (116G) / R-Tile 32G PCIe (CXL) Lanes. **Example:** If an entry in the table below contains 720(360)/16(12)/4(4)/48(48), it means, 720 GPIO of which 360 are LVDS; sixteen 32G NRZ channels or twelve 58G PAM4 channels; Four 58G NRZ channels or four 116G PAM4 channels; forty-eight up to 32G/lane PCIe or forty-eight lanes of CXL

Intel Agilex I-Series Device Names	2957A <sup>(21)</sup>	3179A <sup>(22)</sup>
AGI 022	720(360)/4(4)/0(0)/48(48)	720(360)/48(36)/8(8)/16(16)
AGI 027	720(360)/4(4)/0(0)/48(48)	720(360)/48(36)/8(8)/16(16)

## 1.6. Intel Hyperflex Core Architecture

Intel Agilex FPGAs and SoCs are based on a core fabric featuring the second generation Intel Hyperflex core architecture. The Intel Hyperflex core architecture delivers up to 40% higher clock frequency performance or up to 40% lower power compared to previous generation of high-end Intel FPGAs.

Along with this performance breakthrough, the Intel Hyperflex core architecture delivers a number of advantages including:

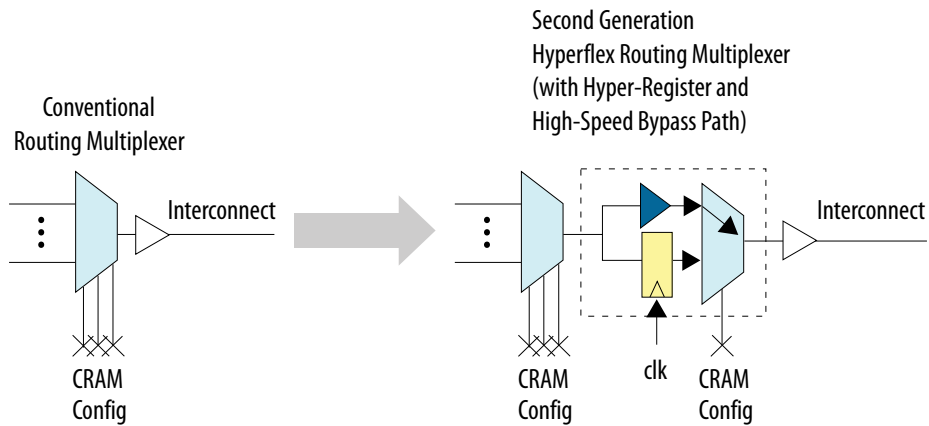
- **Higher Throughput:** Leverages up to 40% higher core clock frequency performance of designs in previous generation high-end FPGAs to obtain throughput breakthroughs
- **Improved Power Efficiency:** Uses reduced IP size enabled by Intel Hyperflex architecture to consolidate designs which previously spanned multiple devices into a single device, thereby reducing power by up to 40% versus previous generation devices
- **Greater Design Functionality:** Uses faster clock frequency to reduce bus widths and reduce IP size, freeing up additional FPGA resources to add greater functionality
- **Increased Designer Productivity:** Boosts performance with less routing congestion and fewer design iterations using Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure

In addition to the traditional user registers found in the Adaptive Logic Modules (ALMs), the Intel Hyperflex core architecture introduces additional bypassable registers distributed throughout the fabric of the FPGA. These additional registers, called Hyper-Registers are available on every interconnect routing segment and at the inputs of all functional blocks. In the second generation Intel Hyperflex core architecture, the number of registers have been optimized to improve both timing closure time and fabric area.

<sup>(21)</sup> (F Tile & R-Tile x 3) (56 mm x 45mm, Hex Mixed 1.0/0.92 mm pitch)

<sup>(22)</sup> (F Tile x 3 & R-Tile ) (56 mm x 45 mm, Hex 0.92mm pitch)

Figure 3. Bypassable Hyper Register

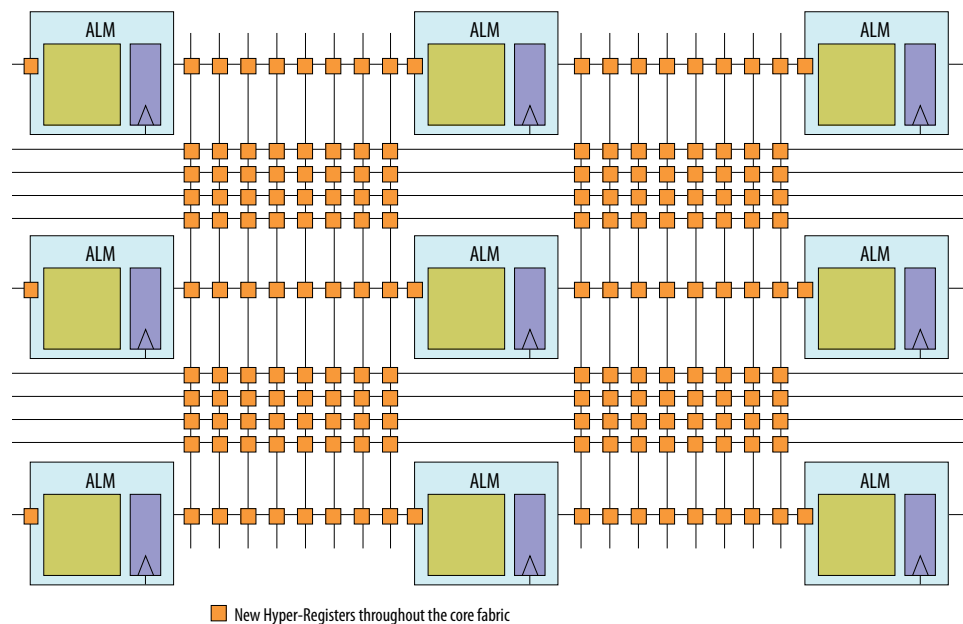


The Hyper-Registers enable the following key design techniques to achieve the up to 40% core performance increases:

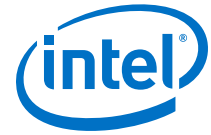
- Fine grain Hyper-Retiming to eliminate critical paths
- Zero latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

By implementing these techniques in your design, the Hyper-Aware design tools automatically make use of the Hyper-Registers to achieve maximum core clock frequency.

Figure 4. Intel Hyperflex Core Architecture



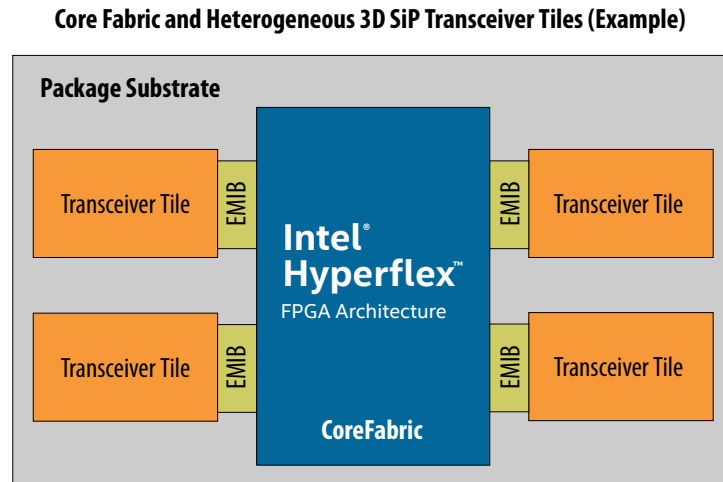




## 1.7. Heterogeneous 3D SiP Transceiver Tile

Intel Agilex FPGAs and SoCs feature power efficient, high bandwidth, low latency transceivers. The transceivers are implemented on heterogeneous 3D System-in-Package (SiP) transceiver tiles. In addition to providing a high-performance transceiver solution to meet current connectivity needs, this allows for future flexibility and scalability as data rates, modulation schemes, and protocol IPs evolve.

**Figure 5. Core Fabric and Heterogeneous 3D SiP Transceiver Tiles**



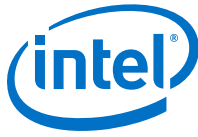
There are five types of transceiver tiles available in Intel Agilex FPGAs:

- E-Tile: General Purpose Transceiver
- P-Tile: PCIe Gen4 Transceiver
- F-Tile: General Purpose and PCIe Gen4 Transceiver
- R-Tile: PCIe Gen5 and Compute Express Link (CXL) Transceiver
- H-Tile: General Purpose and PCIe Gen3 Transceiver

## 1.8. Intel Agilex FPGA Transceivers

Intel Agilex FPGAs offer different transceivers that are optimized for a wide variety of applications, ranging from 1 Gbps to 32 Gbps in NRZ mode and 2 Gbps to 58 Gbps in PAM4 and 116 Gbps PAM4.

The tables below summarize the transceivers capabilities in each tile, and the availability of the tiles in each device family.



**Table 11. Tile Names and Capabilities**

Tile	Maximum Data Rate and Channel Count	Hard IP (HIP)	Applications
E-Tile	12 x 58G PAM4 <i>or</i> 24 x 28.9G NRZ	10/25/100GE MAC, PCS and RSFEC (528,514) , RSFEC (544,514)	General Purpose Transceiver with multi-protocol support for CEI, Ethernet, CPRI, FlexE, Interlaken, Fibre Channel, SRIO, Serial Lite, OTN, JESD204B/C, FlexO, IEEE1588
P-Tile	16 x 16G NRZ	PCIe Gen4 x16 with 8 PF/2K VF SR-IOV EP/RP	PCIe Gen4 x16 including port bifurcation support for 2x8 EP or 4x4 RP, CvP , Autonomous HIP, SR-IOV 8PF / 2kVF, VirtIO, Scalable IOV and Shared Virtual Memory
F-Tile	4 x 116G PAM4 12 x 58G PAM4 <i>or</i> 16 x 32G NRZ	10/25/50/100/200/400GE MAC, PCS, and KR/KP RSFEC PCIe Gen4 x16 with 8 PF/2K VF SR-IOV EP/RP	General Purpose Transceiver with multi-protocol support for CEI, Ethernet, CPRI, FlexE, 600G Interlaken, Fibre Channel, SRIO, Serial Lite, OTN, JESD204B/C, IEEE1588, FlexO, GPON, SDI, Vby1, HDMI, CvP, Display Port P-Tile PCIe features plus Precise Time Management and PMA direct mode
R-Tile	16 x 32G NRZ	PCIe Gen5 x16 with 8 PF/2K VF SR-IOV EP/RP Compute Express Link (CXL)	PCIe Gen5 x16 including port bifurcation support for 2x8 EP or 4x4 RP, CvP, Autonomous HIP, SR-IOV 8PF / 2kVF, VirtIO, Scalable IOV, and Shared Virtual Memory, separate header and payload interfaces on user interface, Precise Time Management, PIPE Direct
H-Tile	16 x 28.3G NRZ 8 x 17.4G NRZ	PCIe - Gen3 x16, SR-IOV (4 Physical Functions, 2K Virtual Functions) Ethernet - 50/100 GbE MAC	General purpose transceivers

**Table 12. Tile Availability in Device Family**

Tile Name	Intel Agilex F-Series FPGAs	Intel Agilex I-Series FPGAs
E-Tile	Y	-
P-Tile	Y	-
F-Tile	Y	Y
R-Tile	-	Y
H-Tile	Y	-

### 1.8.1. E-Tile Transceivers

The E-Tile transceivers provide continuous data rates from 1 Gbps to 28.9 Gbps in NRZ mode and 2 Gbps to 58 Gbps in PAM4 mode. For longer-reach backplane driving applications, advanced adaptive equalization circuits are used to equalize of system loss.

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment and other preprocessing functions before transferring data to the FPGA core fabric.



Within each transceiver tile, the transceivers are arranged as a single PMA-PCS channel with independent clock domains. A wide variety of bonded and non-bonded data rate configurations are possible within each bank, and within each tile, using a highly configurable clock distribution network.

### 1.8.1.1. PMA Features

PMA channels are comprised of transmitter (TX), receiver (RX) and high speed clocking resources.

The transmit features deliver exceptional signal integrity at data rates up to 58 Gbps PAM4 / 28.9 Gbps NRZ.

Each PMA also has advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

**Table 13. Transceiver PMA Features**

Feature	Capability
Data Rates	Up to 58 Gbps
Optical Module Support	XFP, QSFP-DD, OSFP, QSFP/QSFP28, QSFP56, SFP+, SFP28, SFP56, CFP/CFP2/CFP4 optical module support
Cable Driving Support	SFP+ Direct Attach, eSATA
Transmit Pre-Emphasis	One post-tap and three pre-tap for PAM4 One post-tap and one pre-tap for NRZ
Dynamic Reconfiguration	Allows for independent control of each transceiver channel Avalon memory-mapped interface for the most transceiver flexibility
Multiple PCS-PMA and PCS-Core to FPGA fabric interface widths	16, 20, 32, 40 or 64 bit interface widths for flexibility of deserialization width, encoding and reduced latency

### 1.8.1.2. PCS Features

Intel Agilex E-Tile PMA channels interface with core logic through configurable and bypassable PCS interface layers.

The PCS contains multiple gearbox implementations to decouple the PMA and PCS interface widths. This feature provides the flexibility to implement a wide range of applications with 8, 10, 16, 20, 32, 40, or 64-bit interface width between each transceiver and the core logic.

The PCS also contains hard IP to support a variety of standard and proprietary protocols across a wide range of data rates and encoding schemes. The Standard PCS mode provides support for 8B/10B encoded applications up to 12.5 Gbps. The Enhanced PCS mode supports 64B/66B and 64B/67B encoded applications up to 58 Gbps. The enhanced PCS mode also includes an integrated KP and KR Forward Error Correction (FEC) circuit. For highly customized implementations, a PCS Direct mode provides an interface up to 64 bits wide to allow for custom encoding and support for data rates up to 28.9 Gbps.

## 1.8.2. P-Tile Transceivers

The Intel Agilex P-Tile transceivers are exclusively used for PCIe and support up to Gen4 x16 at 16 Gbps data rates. It contains the following features:



- Port bifurcation support: 2x8 Endpoint or 4x4 Rootport
- TL Bypass features
- CvP
- Autonomous Hard IP
- SR-IOV 8 PF / 2 kVF
- VirtIO support
- Scalable IOV
- Shared Virtual Memory

### 1.8.3. F-Tile Transceivers

The Intel Agilex F-Tile transceivers are general purpose transceivers with the following speed options:

- 4 channels at 116G NRZ/PAM4
- 12 channels at 58G PAM4 or 16 channels at 32G NRZ

It has multi-protocol support for CEI, Ethernet, CPRI, FlexE, 600G Interlaken, Fibre Channel, SRIO, SerialLite IV, OTN, JESD204B/C, FlexO, IEEE1588, GPON, SDI, Vby1, HDMI, Display Port.

In addition, F-Tile has PCIe Gen4 x16 support with P-Tile feature set plus Precise Time Management and PMA direct mode.

### 1.8.4. R-Tile Transceivers

The Intel Agilex R-Tile transceivers are used for PCIe and support up to Gen5 x16 at 32G data rates. They contain the following features:

- Port bifurcation support: 2x8 Endpoint or 4x4 Rootport
- TL Bypass Feature
- CvP
- Autonomous Hard IP
- Separate header and payload interfaces on user interface
- SR-IOV 8 PF / 2 kVF
- VirtIO support
- Scalable IOV
- Shared Virtual Memory
- Precise Time Management
- PIPE Direct

In addition, the R-Tile contains hardened Compute Express Link (CXL) IP.

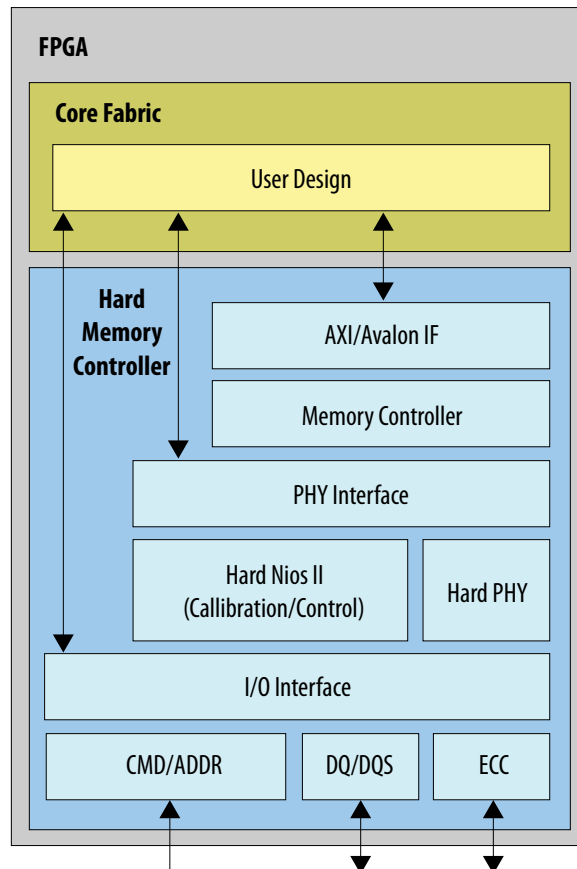
## 1.9. External Memory and General Purpose I/O

Intel Agilex devices offer substantial external memory bandwidth, with up to five 72-bit wide DDR4 memory interfaces running at up to 3200 Mbps.



This bandwidth is provided along with the ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers. The external memory interfaces can be configured up to a maximum width of 72 bits when using either hard or soft memory controllers.

**Figure 6. Hard Memory Controller**



Each I/O bank contains 96 general purpose I/Os and two high-efficiency hard memory controllers capable of supporting many different memory types, each with different performance capabilities. The hard memory controller is also capable of being bypassed and replaced by a soft controller implemented in the user logic. The I/Os each have a hardened double data rate (DDR) read/write path (PHY) capable of performing key memory interface functionality such as:

- Read/Write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

The timing calibration is aided by the inclusion of hard microcontrollers based on Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Agilix device to compensate for any

changes in process, voltage, or temperature either within the Intel Agilex device itself or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

**Table 14. External Memory Interface Performance**

External Memory Interface	Memory Controller Type	Performance
DDR4	Hard	3200 Mbps
DDR5 <sup>(23)</sup>	Hard	4400 Mbps
QDRIV	Soft	2133 Mbps
RLDRAM III	Soft	2400 Mbps

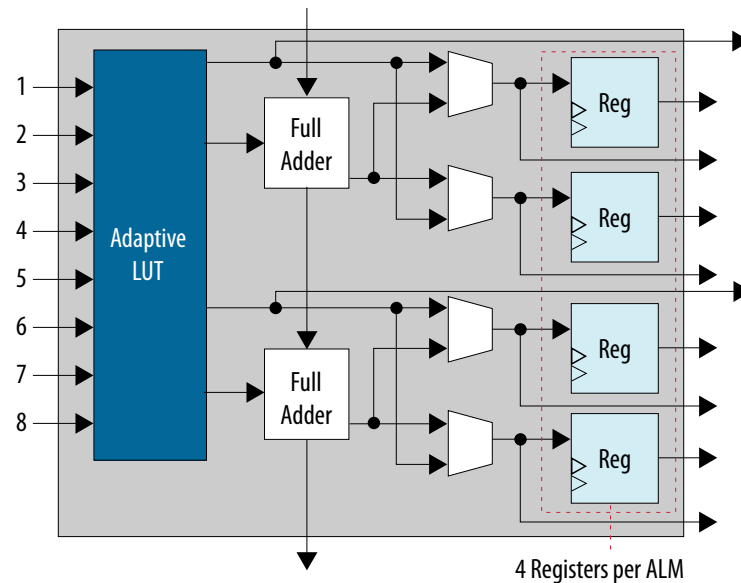
Intel Agilex devices also feature general purpose I/Os capable of supporting a wide range of single-ended and differential I/O interfaces, including 1.5 V true differential signaling compatible with LVDS/ RSDS/ Mini-LVDS/ LVPECL. The LVDS compatible solution rates up to 1.6 Gbps are supported.

### 1.10. Adaptive Logic Module (ALM)

Intel Agilex devices use an enhanced adaptive logic module (ALM) similar to the previous generation Intel Stratix® 10 and Intel Arria® 10 FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the devices.

The ALM block diagram shown in the following figure has eight inputs with fracturable look-up table (LUT), two dedicated embedded adders and four dedicated registers.

**Figure 7. ALM Block Diagram**



Key features and capabilities of the ALM include:

<sup>(23)</sup> DDR5 supported in Intel Agilex M-series devices only



- High register count with 4 registers per 8-input fracturable LUT, operating in conjunction with the second generation Intel Hyperflex architecture enables Intel Agilex devices to maximize core performance at very high core logic utilization
- Implements select 7-input logic functions, all 6-input logic functions and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core logic utilization
- New in Intel Agilex ALM architecture are two clock sources for each ALM which generate two normal clocks and two delayed clocks to drive the ALM registers; resulting in more clock domains and time-borrowing capability
- Additional fast 6 LUT and 5 LUT outputs for combinatorial functions; resulting in improved critical path for cascade of logic
- Improved register packing mode, including 5-input LUT with 2 packed register paths resulting in more efficient usage of the fabric area leading to improved critical path
- New support for latch mode in the address latch enable

The Intel Quartus Prime software leverages the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Intel Quartus Prime software simplifies design reuse as it automatically maps legacy designs into the Intel Agilex FPGA's ALM architecture.

### 1.11. Core Clock Network

Core clocking function in Intel Agilex devices employs the use of programmable clock tree synthesis.

This technique uses dedicated clock tree routing and switching circuits, and allows the Intel Quartus Prime software to create the exact clock trees required for your design. Clock tree synthesis minimizes clock tree insertion delay, reduces dynamic power dissipation in the clock tree and allows greater clocking flexibility in the core while still maintaining backwards compatibility with legacy global and regional clocking schemes.

The core clock network in Intel Agilex devices supports the second generation Intel Hyperflex core architecture. It also supports the hard memory controllers up to 3200 Mbps for DDR4 with a quarter rate transfer to the core. The core clock network is supported by dedicated clock input pins and integer I/O PLLs.

### 1.12. I/O PLLs

Intel Agilex FPGAs contain I/O PLLs available for general purpose use in the core fabric and for simplifying the design of external memory interfaces and high-speed LVDS interfaces. The I/O PLLs are located adjacent to the hard memory controllers and LVDS serializer/deserializer (SERDES) blocks in the I/O banks. Each I/O bank contains two I/O Bank I/O PLLs and one fabric-feeding I/O PLL. This placement makes it easier to close timing because the I/O PLLs are tightly coupled with the I/Os that need to use them. The I/O PLLs can be used for general purpose applications in the core such as clock network delay compensation and zero-delay clock buffering.

### 1.13. Internal Embedded Memory

Intel Agilex devices contain three types of embedded memory blocks:



- MLAB (640 bits)
- M20K (20 Kbits)
- eSRAM (18 Mbits)

The M20K and MLAB blocks are familiar block sizes carried over from previous Intel device families. The MLAB blocks are ideal for wide and shallow memories, while the M20K blocks are intended to support larger memory configurations and include hard ECC. Both M20K and MLAB internal embedded memory blocks can be configured as a single-port or dual-port RAM, FIFO, ROM, or shift register.

In addition, some Intel Agilex devices also include 18 Megabit (Mb) eSRAM blocks with stitching support. These blocks are large size, fast path, low latency, high bandwidth on-chip memory block and include ECC.

These memory blocks are highly flexible and support a number of memory configurations as shown in the table below.

**Table 15. Internal Embedded Memory Block Configuration**

MLAB (640 bits)	M20K (20 Kbits)	eSRAM (18 Mbits)
64 x 10 (supported through emulation) 32 x 20	2K x 10 (or x8) 1K x 20 (or x 16) 512 x 40 (or x32)	8 channels of 2.25Mb (18Mb) (each channel contains 32 banks of 72 x 1K memory)

## 1.14. Variable Precision DSP

The Intel Agilex FPGAs' DSP blocks are based upon the variable precision DSP Architecture used in Intel's previous generation devices. They feature hard fixed point and IEEE-754 compliant floating point capability which includes single-precision (32-bit arithmetic) FP32 floating point mode. New to Intel Agilex FPGAs is the support for half-precision (16-bit arithmetic) FP16 floating point modes and BFLOAT16 floating-point format. The number of 9x9 multipliers have also increased, with two 9x9 multipliers for every one 18x19 multiplier, as compared to the previous generation of FPGAs.

The DSP blocks can be configured to support signal processing with precision ranging from 9x9 up to 54x54. A pipeline register has been added to increase the maximum operating frequency of the DSP block and reduce power consumption. In addition, dynamic switching of inputs to the multiplier is available through `scanin` and `chainout` features.



Figure 8. Low Precision Fixed Point Mode

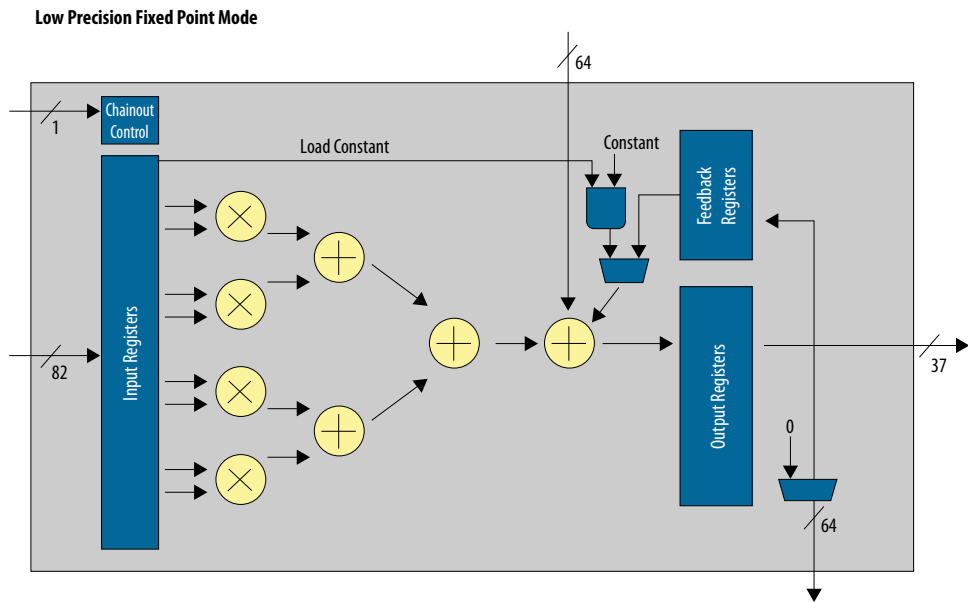


Figure 9. Standard Precision Fixed Point Mode

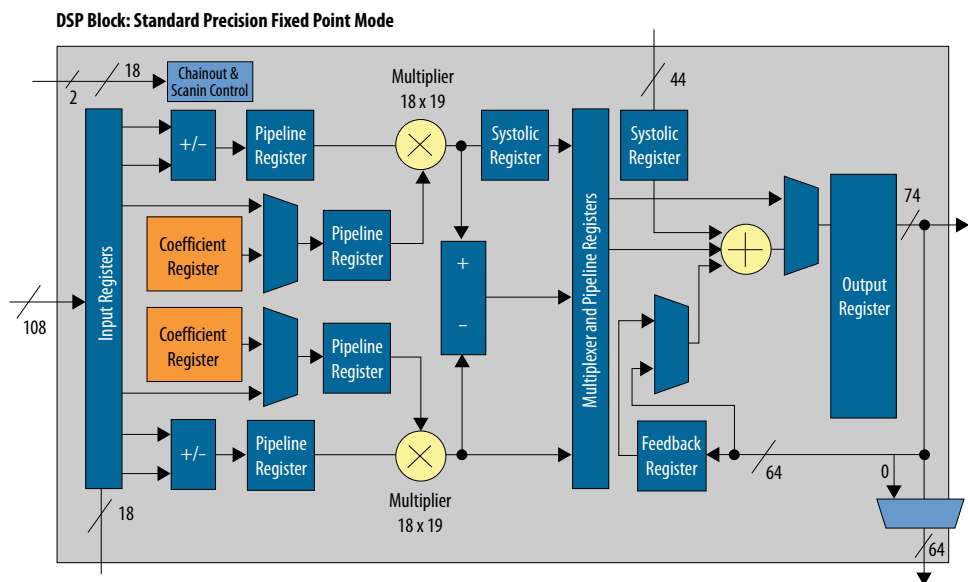


Figure 10. High Precision Fixed Point Mode

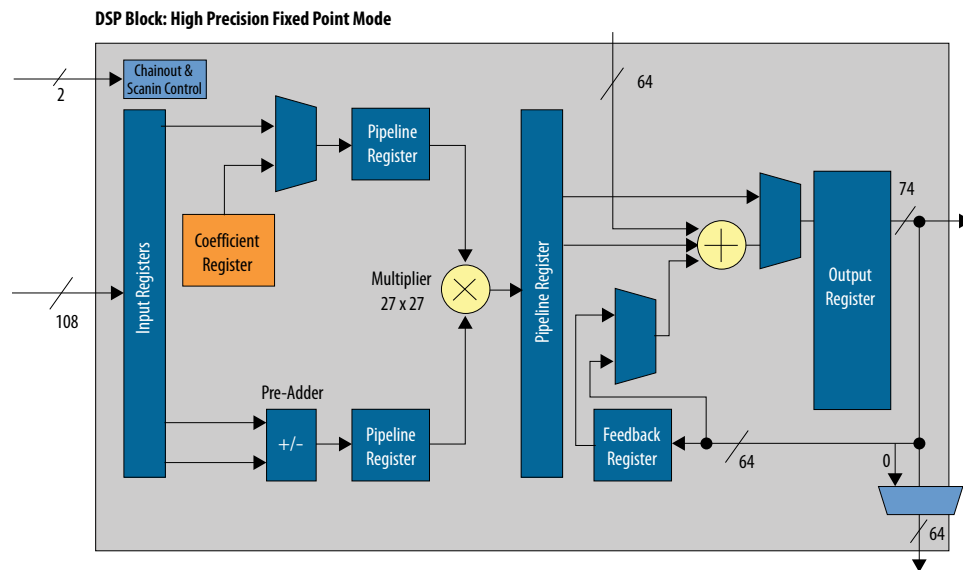
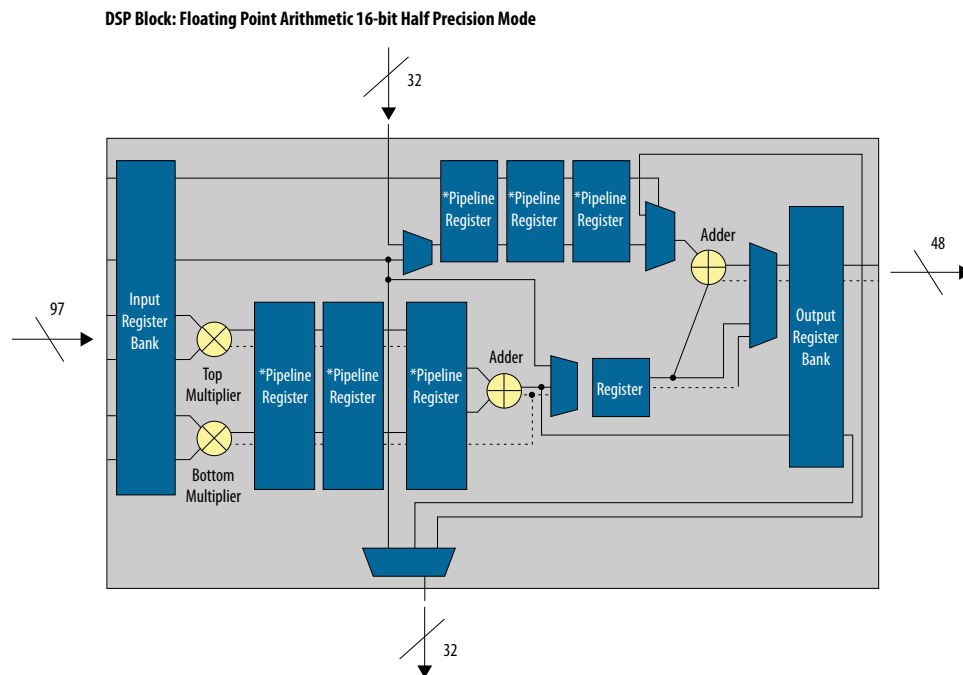


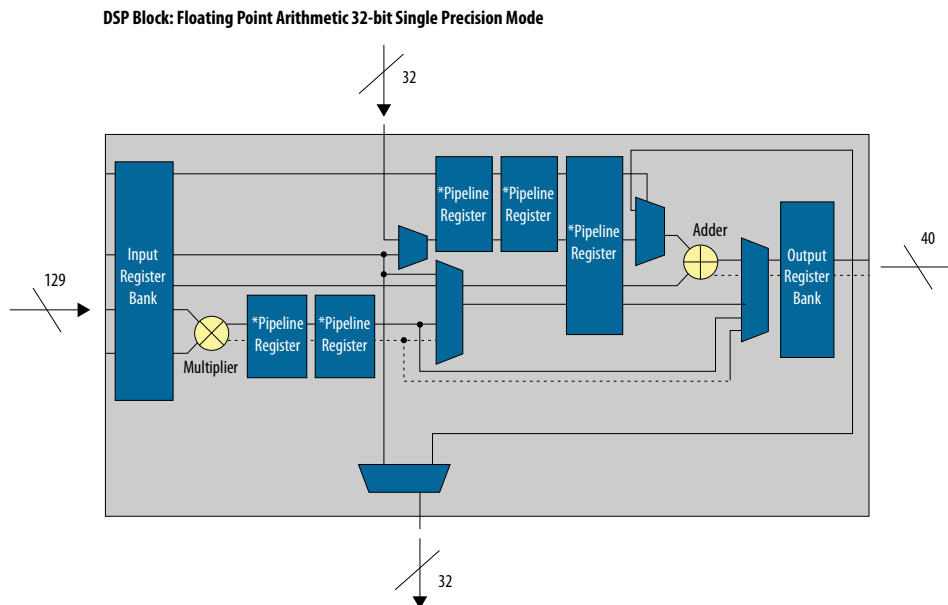
Figure 11. Half Precision Floating Point Arithmetic 16-bit



\*This block diagram shows the functional representation of the DSP block. The pipeline registers are embedded within the various circuits of the DSP block.



**Figure 12. Single Precision Floating Point Arithmetic 32-bit**



\*This block diagram shows the functional representation of the DSP block. The pipeline registers are embedded within the various circuits of the DSP block.

Each DSP block can be independently configured at compile time as either quad 9x9, dual 18x19 or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, multiple variable precision DSP blocks can be cascaded to implement even higher precision DSP functions efficiently.

In floating point mode, each DSP block provides either single precision or half precision floating point (including FP16 and BFLOAT16) multiplier and adder. Floating point additions, multiplications, mult-adds and multaccumulates are supported.

The following table shows how different precisions are accommodated within a DSP block, or by utilizing multiple blocks.

**Table 16. Variable Precision DSP Block Configuration**

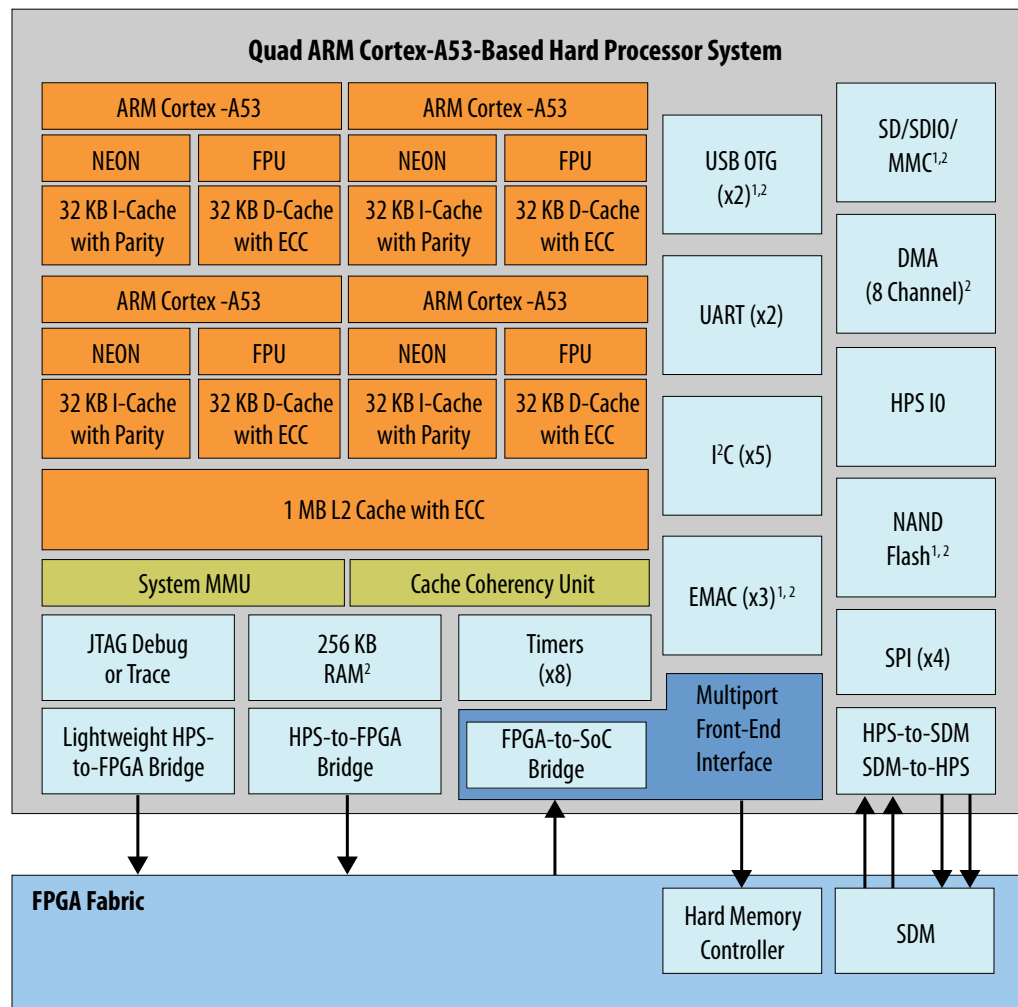
Multiplier Size	DSP Block Resources	Expected Usage
9x9 bits	1/4 of Variable Precision DSP Block	Low precision fixed point
18x19 bits	1/2 of Variable Precision DSP Block	Medium precision fixed point
27x27 bits	1 Variable Precision DSP Block	High precision fixed point
19x36 bits	1 Variable Precision DSP Block with external adder	Fixed point FFT
36x36 bits	2 Variable Precision DSP Blocks with external adder	Very high precision fixed point
54x54 bits	4 Variable Precision DSP Blocks with external adder	Double precision fixed point
Half Precision floating Point	1 variable precision DSP block (contains adder for two FP16 multipliers plus an accumulator)	Half Precision Floating point
Single Precision floating point	1 variable precision DSP block (contains one FP32 multipliers with an accumulator)	Single Precision Floating point

### 1.15. Hard Processor System (HPS)

The Intel Agilex SoC Hard Processor System (HPS) is Intel’s industry leading third generation HPS. The HPS is a quad-core Arm Cortex-A53, which allows users to easily migrate existing SoC designs from Intel Stratix 10 SoCs to Intel Agilex SoC.

The HPS also enables system-wide hardware virtualization capabilities by adding a system memory management unit. These architecture improvements ensure that SoCs meet the requirements of current and future embedded markets, including wireless and wireline communications, data center acceleration, and numerous military applications.

Figure 13. HPS Block Diagram



- Notes:
1. Integrated direct memory access (DMA)
  2. Integrated error correction code (ECC)



## Key Features of the Intel Agilex HPS

**Table 17. Key Feature Summary**

Feature	Description
<b>Quad-core ARM Cortex-A53 MPCore processor unit</b>	<ul style="list-style-type: none"> <li>• 2.3 MIPS/MHz instruction efficiency</li> <li>• CPU frequency up to 1.4 GHz</li> <li>• At 1.4 GHz total performance of 13,800 MIPS</li> <li>• ARMv8-A architecture</li> <li>• Runs 64-bit and 32-bit ARM instructions</li> <li>• 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint</li> <li>• Jazelle® RCT execution architecture with 8-bit Java bytecodes</li> <li>• Superscalar, variable length, out-of-order pipeline with dynamic branch prediction</li> <li>• Improved ARM NEON media processing engine</li> <li>• Single and double-precision floating-point unit</li> <li>• CoreSight debug and trace technology</li> </ul>
<b>System Memory Management Unit</b>	<ul style="list-style-type: none"> <li>• Enables a unified memory model and extends hardware virtualization into peripherals implemented in the FPGA fabric</li> </ul>
<b>Cache Coherency Unit</b>	<ul style="list-style-type: none"> <li>• Changes in shared data stored in cache are propagated throughout the system providing bi-directional coherency for co-processing elements.</li> </ul>
<b>Cache Memory</b>	<ul style="list-style-type: none"> <li>• <b>L1 Cache</b> <ul style="list-style-type: none"> <li>– 32 KB of instruction cache with parity check</li> <li>– 32 KB of L1 data cache with ECC</li> <li>– Parity checking</li> </ul> </li> <li>• <b>L2 Cache</b> <ul style="list-style-type: none"> <li>– 1 MB shared</li> <li>– 8-way set associative</li> <li>– SEU Protection with parity on TAG ram and ECC on data RAM</li> <li>– Cache lockdown support</li> </ul> </li> </ul>
<b>On-Chip Memory</b>	<ul style="list-style-type: none"> <li>• 256 KB of scratch on-chip RAM</li> </ul>
<b>External SDRAM and Flash Memory Interfaces for HPS</b>	<ul style="list-style-type: none"> <li>• <b>Hard memory controller with support for DDR4</b> <ul style="list-style-type: none"> <li>– 40-bit (32-bit + 8 bit ECC) with select packages supporting 72-bit (64 bit + 8 bit ECC)</li> <li>– Support for up to 3200 Mbps DDR4</li> <li>– Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters</li> <li>– Software Configurable Priority Scheduling on individual SDRAM bursts</li> <li>– Fully programmable timing parameter support for all JEDEC-specified timing parameters</li> <li>– Multiport front-end (MPFE) scheduler interface to the hard memory controller, which supports the AXI® Quality of Service (QoS) for interface to the FPGA fabric</li> </ul> </li> <li>• <b>NAND flash controller</b> <ul style="list-style-type: none"> <li>– ONFI 1.0</li> <li>– Integrated descriptor based with DMA</li> <li>– Programmable hardware ECC support</li> <li>– Support for 8 and 16 bit Flash devices</li> </ul> </li> <li>• <b>Secure Digital SD/SDIO/MMC controller</b> <ul style="list-style-type: none"> <li>– eMMC 4.5</li> <li>– Integrated descriptor based DMA</li> <li>– CE-ATA digital commands supported</li> <li>– 50 MHz operating frequency</li> </ul> </li> <li>• <b>Direct memory access (DMA) controller</b> <ul style="list-style-type: none"> <li>– 8-channel</li> <li>– Supports up to 32 peripheral handshake interface</li> </ul> </li> </ul>

*continued...*



Feature	Description
<b>Communication Interface Controllers</b>	<ul style="list-style-type: none"> <li>• <b>Three 10/100/1000 Ethernet media access controls (MAC) with integrated DMA</b> <ul style="list-style-type: none"> <li>– Supports RGMII and RMII external PHY Interfaces</li> <li>– Option to support other PHY interfaces through FPGA logic               <ul style="list-style-type: none"> <li>• GMII</li> <li>• MII</li> <li>• RMII (requires MII to RMII adapter)</li> <li>• RGMII (requires GMII to RGMII adapter)</li> <li>• SGMII (requires GMII to SGMII adapter)</li> </ul> </li> <li>– Supports IEEE 1588-2002 and IEEE 1588-2008 standards for precision networked clock synchronization</li> <li>– Supports IEEE 802.1Q VLAN tag detection for reception frames</li> <li>– Supports Ethernet AVB standard</li> </ul> </li> <li>• <b>Two USB On-the-Go (OTG) controllers with DMA</b> <ul style="list-style-type: none"> <li>– Dual-Role Device (device and host functions)               <ul style="list-style-type: none"> <li>• High-speed (480 Mbps)</li> <li>• Full-speed (12 Mbps)</li> <li>• Low-speed (1.5 Mbps)</li> <li>• Supports USB 1.1 (full-speed and low-speed)</li> </ul> </li> <li>– Integrated descriptor-based scatter-gather DMA</li> <li>– Support for external ULPI PHY</li> <li>– Up to 16 bidirectional endpoints, including control endpoint</li> <li>– Up to 16 host channels</li> <li>– Supports generic root hub</li> <li>– Configurable to OTG 1.3 and OTG 2.0 modes</li> </ul> </li> <li>• <b>Five I<sup>2</sup>C controllers (three can be used by EMAC for MIO to external PHY)</b> <ul style="list-style-type: none"> <li>– Support both 100 Kbps and 400 Kbps modes</li> <li>– Support both 7 bit and 10 bit addressing modes</li> <li>– Support Master and Slave operating mode</li> </ul> </li> <li>• <b>Two UART 16550 compatible</b> <ul style="list-style-type: none"> <li>– Programmable baud rate up to 115.2 Kbaud</li> </ul> </li> <li>• <b>Four serial peripheral interfaces (SPI) (2 Masters, 2 Slaves)</b> <ul style="list-style-type: none"> <li>– Full and Half duplex</li> </ul> </li> </ul>
<b>Timers and I/O</b>	<ul style="list-style-type: none"> <li>• <b>Timers</b> <ul style="list-style-type: none"> <li>– 4 general-purpose timers</li> <li>– 4 watchdog timers</li> </ul> </li> <li>• 48 HPS direct I/O allow HPS peripherals to connect directly to I/O</li> <li>• Up to two IO96 banks may be assigned to HPS for HPS DDR access</li> </ul>
<b>Interconnect to Logic Core</b>	<ul style="list-style-type: none"> <li>• <b>HPS-to-FPGA Bridge</b> <ul style="list-style-type: none"> <li>– Allows HPS bus masters to access bus slaves in FPGA fabric</li> <li>– Configurable 32, 64, or 128 bit AMBA AXI interface allows high-bandwidth HPS master transactions to FPGA fabric</li> </ul> </li> <li>• <b>HPS-to-SDM and SDM-to-HPS Bridges</b> <ul style="list-style-type: none"> <li>– Allows the HPS to reach the SDM block and the SDM to bootstrap the HPS</li> </ul> </li> <li>• <b>Light Weight HPS-to-FPGA Bridge</b> <ul style="list-style-type: none"> <li>– Light weight 32 bit AXI interface suitable for low-latency register accesses from HPS to soft peripherals in FPGA fabric</li> </ul> </li> <li>• <b>FPGA-to-SoC Bridge</b> <ul style="list-style-type: none"> <li>– Configurable 128, 256, 512 bit ACE-Lite interface</li> <li>– Up to 256-bit FPGA-to-SoC targeting HPS</li> <li>– Up to 512-bit FPGA-to-SoC targeting DDR</li> </ul> </li> </ul>



## 1.16. Power Management

Intel Agilex devices leverage the advanced Intel 10-nm FinFET process technology, the second generation Intel Hyperflex core architecture, power gating, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to previous generation high-performance Intel Stratix 10 devices.

Intel Agilex standard power devices (-V) are SmartVID devices. The core voltage supplies (VCC and VCCP) for each SmartVID device must be driven by a PMBus voltage regulator dedicated to that Intel Agilex device. Use of a PMBus voltage regulator for each SmartVID (-V) device is mandatory; not optional. A code is programmed into each SmartVID device during manufacturing that allows the PMBus voltage regulator to operate at the optimum core voltage to meet the device performance specifications. There are Intel Agilex device options available that used a fixed core voltage. These devices are designated (-F) and are available with limited core speed options.

Additionally, power gating reduces static power of unused resources in the FPGA by powering them down. The Intel Quartus Prime software automatically powers down specific unused resource blocks such as DSP and M20K blocks at configuration time.

The optional power reduction techniques in Intel Agilex devices include:

- **Low Static Power Devices:** Intel Agilex devices are available that provide lower static power than the SmartVID standard power devices, while maintaining device performance

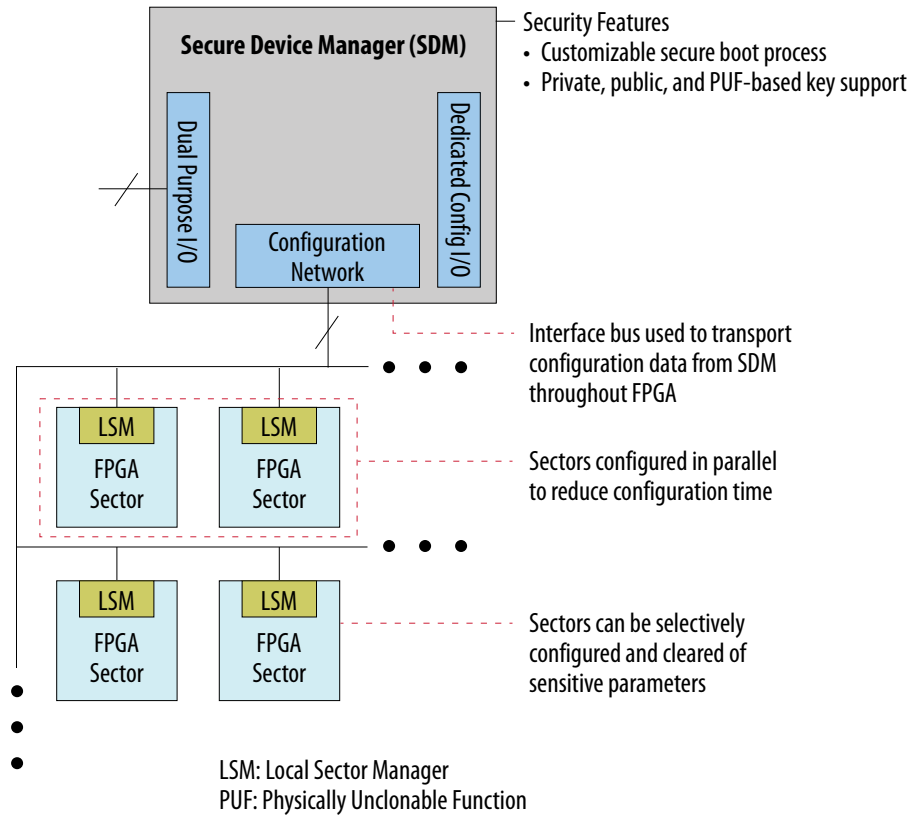
Furthermore, Intel Agilex devices features industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 50% less power than the equivalent soft logic implementations.

## 1.17. Device Configuration and Secure Device Manager (SDM)

All Intel Agilex devices contain a Secure Device Manager (SDM), which is a dedicated triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. The SDM also bootstraps the HPS in SoC devices ensuring that the HPS can boot using the same security features that the FPGA devices have.

Figure 14. SDM Block Diagram

SDM Block Diagram



During configuration, Intel Agilex devices are divided into logical sectors, each of which is managed by a local sector manager (LSM). The SDM passes configuration data to each of the LSMs across the on-chip configuration network. This allows the sectors to be configured independently, one at a time, or in parallel. This approach achieves simplified sector configuration and reconfiguration, as well as reduced overall configuration time due to the inherent parallelism. The same sector-based approach is used to respond to single-event upsets and security attacks.

While the sectors provide a logical separation for device configuration and reconfiguration, they overlay the normal rows and columns of FPGA logic and routing. This means there is no impact to the Intel Quartus Prime software place and route, and no impact to the timing of logic signals that cross the sector boundaries.

The SDM enables robust, secure, fully-authenticated device configuration. It also allows for customization of the configuration scheme, which can enhance device security. For configuration and reconfiguration, this approach offers a variety of advantages:

- Dedicated secure configuration manager
- Reduced device configuration time, because sectors are configured in parallel
- Updateable configuration process





- Partial Reconfiguration
- Remote System Update
- Zeroization of individual sectors or the complete device

The SDM also provides additional capabilities such as register state readback and writeback to support ASIC prototyping and other applications.

## 1.18. Device Security

Building on top of the robust security features present in the previous generation devices, Intel Agilex FPGAs and SoCs include a number of new and innovative security enhancements. These features are also managed by the SDM, tightly coupling device configuration and reconfiguration with encryption, authentication, key storage and anti-tamper services.

Security services provided by the SDM include:

- Bitstream encryption
- Multi-factor authentication
- Hard encryption and authentication acceleration; AES-256, SHA-256/384, ECDSA-256/384
- Volatile and non-volatile encryption key storage and management
- Physically Unclonable Function (PUF) service
- Updateable configuration process
- Secure device maintenance and upgrade functions
- Side-channel attack protection
- Scripted response to sensor inputs and security attacks, including selective sector zeroization
- Readback, JTAG and test mode disable
- Enhanced response to single-event upsets (SEU)
- Platform Attestation

## 1.19. CvP Using PCI Express

Configuration via protocol using PCI Express allows the Intel Agilex FPGA to be configured across the PCI Express bus, simplifying the board layout and increasing system integration. Making use of the embedded PCI Express hard IP operating in autonomous mode before the FPGA is configured allows the PCI Express bus to be powered up and active within the 100 ms time allowed by the PCI Express specification. Intel Agilex FPGA devices also support partial reconfiguration across the PCI Express bus which reduces system down time by keeping the PCI Express link active while the device is being reconfigured.

## 1.20. Partial and Dynamic Configuration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue running. This capability is required in systems where uptime is critical, because it allows you to make updates or adjust functionality without disrupting services.



In addition to lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place in the FPGA those functions that do not operate simultaneously. Instead, these functions can be stored in external memory and loaded as needed. This reduces the size of the required FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power. The partial reconfiguration process is built on top of the proven incremental compile design flow in the Intel Quartus Prime design software.

Dynamic reconfiguration in Intel Agilex devices allows transceiver data rates, protocols and analog settings to be changed dynamically on a channel-by-channel basis while maintaining data transfer on adjacent transceiver channels. Dynamic reconfiguration is ideal for applications that require on-the-fly multiprotocol or multi-rate support. Both the PMA and PCS blocks within the transceiver can be reconfigured using this technique. Dynamic reconfiguration of the transceivers can be used in conjunction with partial reconfiguration of the FPGA to enable partial reconfiguration of both core and transceivers simultaneously.

### 1.21. Fast Forward Compile

The innovative Fast Forward Compile feature in the Intel Quartus Prime software identifies performance bottlenecks in your design and provides detailed, step-by-step performance improvement recommendations that you can then implement. The compiler report estimates of the maximum operating frequency that can be achieved by applying the recommendations. As part of the new Hyper-Aware design flow, Fast Forward Compile maximizes the performance of your Intel Agilex design and achieves rapid timing closure.

Previously, this type of optimization required multiple time-consuming design iterations, including full design re-compilation to determine the effectiveness of the changes. Fast Forward Compile enables you to make better decisions about where to focus your optimization efforts, and how to increase your design performance and throughput. This technique removes much of the guesswork of performance exploration, resulting in fewer design iterations and as much as up to 40% higher core performance gains for Intel Agilex designs.

### 1.22. Single Event Upset (SEU) Error Detection and Correction

Intel Agilex FPGAs and SoCs offer robust SEU error detection and correction circuitry. The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running parity checker circuit with integrated ECC that automatically corrects one or two bit errors and detects higher order multibit errors.

The physical layout of the CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the user memories also include integrated ECC circuitry and are layout optimized for error detection and correction.



The SEU error detection and correction hardware is supported by both soft IP and the Intel Quartus Prime software to provide a complete SEU mitigation solution. The components of the complete solution include:

- Hard error detection and correction for CRAM and user M20K memory blocks
- Optimized physical layout of memory cells to minimize probability of SEU
- Sensitivity processing soft IP that reports if CRAM upset affects a used or unused bit
- Fault injection soft IP with the Intel Quartus Prime software support that changes state of CRAM bits for testing purposes
- Hierarchy tagging in the Intel Quartus Prime software
- Triple Mode Redundancy (TMR) used for the Secure Device Manager and critical on-chip state machines

In addition to the SEU mitigation features listed above, the Intel 10-nm FinFET process technology used for Intel Agilex devices is based on FinFET transistors which have reduced SEU susceptibility versus conventional planar transistors.

### **1.23. Additional Information**

For latest information about Intel Agilex devices, please visit Intel Agilex product page on Intel's website.

#### **Related Information**

[Intel Agilex Product Page](#)



## 2. Revision History

**Table 18. Revision History for the Intel Agilex FPGAs and SoCs Advanced Information Brief**

Document Version	Changes
2020.09.30	Sections Updated: <ul style="list-style-type: none"> <li>• <a href="#">Intel® Agilex™ FPGA and SoC Device Overview</a> on page 3</li> <li>• <a href="#">Intel Agilex FPGA and SoC Summary of Features</a> on page 6</li> <li>• <a href="#">Intel Agilex FPGA and SoC Family Plan</a> on page 11</li> <li>• <a href="#">Intel Hyperflex Core Architecture</a> on page 15</li> <li>• <a href="#">Intel Agilex FPGA Transceivers</a> on page 17</li> </ul>
2019.07.02	Sections Updated: <ul style="list-style-type: none"> <li>• <a href="#">Intel® Agilex™ FPGA and SoC Device Overview</a> on page 3</li> <li>• <a href="#">Intel Agilex FPGA and SoC Family Variants</a> on page 5</li> <li>• <a href="#">Intel Agilex F-Series SoC FPGAs</a> on page 5</li> <li>• <a href="#">Intel Agilex I-Series SoC FPGAs</a> on page 5</li> <li>• <a href="#">Intel Agilex M-Series SoC FPGAs</a> on page 5</li> <li>• <a href="#">Common Features</a> on page 5</li> <li>• <a href="#">Available Options</a> on page 6</li> <li>• <a href="#">Intel Agilex FPGA and SoC Summary of Features</a> on page 6</li> <li>• <a href="#">Intel Agilex FPGA and SoC Family Plan</a> on page 11</li> <li>• <a href="#">Intel Hyperflex Core Architecture</a> on page 15</li> <li>• <a href="#">Heterogeneous 3D SiP Transceiver Tile</a> on page 17</li> <li>• <a href="#">PCS Features</a> on page 19</li> <li>• <a href="#">P-Tile Transceivers</a> on page 19</li> <li>• <a href="#">External Memory and General Purpose I/O</a> on page 20</li> <li>• <a href="#">Adaptive Logic Module (ALM)</a> on page 22</li> <li>• <a href="#">Internal Embedded Memory</a> on page 23</li> <li>• <a href="#">Variable Precision DSP</a> on page 24</li> <li>• <a href="#">Device Security</a> on page 33</li> </ul>
2019.04.02	Initial Release

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