# Impact of Power-Off Sequencing on SoC FPGA-based Systems

## Introduction

A system's power budget is an important aspect of the design, and Altera SoC FPGAs are designed with power-saving features to minimize power consumption and power supply cost. In addition to including separate processor and FPGA power planes, the power sequencing in Altera SoC FPGAs is designed to be reliable and flexible.

This Architecture Brief examines how Altera's flexible power-off sequencing facilitates reliable, energy-saving operation without the complicated requirements demanded by other vendors' SoCs.

**Key aspects of this Architecture Brief are highlighted in an online video: "Savings Across the Board", which can be found at www.altera.com/socarchitecture in the "Cost and Power" section.**

## Power-Saving Features

Altera SoC FPGAs employ a variety of power-saving features. Separate and independent power planes enable the processor to save power by placing the FPGA, which consumes the majority of the power budget, in a low-power mode, via software control. Other power-saving features are the ability to turn off clocks to unused functions, placing the processor in a sleep mode to wake using an interrupt and utilizing low power modes for key peripherals such as Ethernet and USB.

## Power On/Off Sequencing Requirements

In order to preserve device reliability or guarantee certain power-up states, silicon vendors may provide specific power-on and power-off sequencing requirements as outlined in Table 1, below. While power-on sequencing requirements are fairly common, power-off specifications are rare as a means of protecting the device. The implication is that additional circuitry must be added to the power supply, or the system manufacturer could face long-term reliability concerns.

For devices with power-off sequencing requirements, precautions must be taken to avoid the failure of an individual power rail, which will cause a violation of the specifications. This requires comparative analog circuitry to monitor the rails, and appropriate protective circuitry must be added. To ensure the proper power-off sequence, sufficient energy storage must also be supplied in the event of an unwanted or unexpected external power failure in addition to normal power down circumstances.

There are no sequencing requirements for Altera SoC FPGAs. Internal device protection allows any order of power-on and power-off sequencing. However, Altera provides a recommended power-on sequence, as a guide to system power supply designers to help minimize power supply cost, but it does not have any reliability implications. Vendor B's SoC FPGAs, on the other hand, require power rails to be applied and disconnected, in a specific order. Repeatedly violating these power-on and power-off sequencing requirements can lead to long-term reliability concerns for the device. This places a risk factor on the SoC's power management that is not present with Altera SoC FPGAs.

Altera SoC FPGAs are built with internal device protection such that any order of power-on or power-off sequencing is accepted. They are also guaranteed to bring up I/Os in tri-state, avoiding potential board level driver collisions, avoiding any board-level driver contention. Other SoC FPGA vendor devices cannot guarantee this if power-on sequencing requirements are violated which may cause board-level signal contention.

Furthermore, Altera SoC FPGAs support "hot socketing," where the device can be inserted into a board that is already under power. This functionality is not specified from other SoC FPGA vendors.

### Table 1: SoC FPGA Power-On and Power-Off Sequencing Requirements

| Function/Feature | Altera SoC FPGA | Vendor B |
|---|---|---|
| Power-On Sequence | None | Sequencing is required when I/O banks drive 3.3 V peripherals, in order to maintain device reliability |
| Power-on Sequence for I/O Bring-Up in Tri- State | None | Power-on sequence is required to assure I/Os come up in tri-state |
| Power-Off Sequence | None | Sequencing is required when I/O banks drive 3.3 V peripherals, in order to maintain device reliability |
| Hot Socketing Capability | Yes | Not specified |

## System Cost Implications

Though many sophisticated power management chips are available today which can support both power-on and power-off sequencing, those chips are likely to be more expensive. In addition to the power management chips, additional energy storage may be necessary to provide a controlled power down sequence in the event of an unanticipated or undesired power loss. Monitoring circuitry must also be added to detect and avoid the failure of an individual power rail as mentioned earlier. Thus, implementing a comprehensive power-off sequencing solution can have a noticeable impact to the system bill-of-materials (BOM).

## Conclusion

Altera's SoC FPGAs eliminate the need for power sequencing, which is necessary in other vendors' SoCs. Additionally, Altera SoC FPGAs offer internal device protection, hot socketing support and protection against abrupt power interruption, which all have positive benefits for component count, board area and reliability. Ultimately, the lack of a specific power-off sequencing requirement can help save on overall system cost.

## Want to Dig Deeper?

Explore power savings options with the Altera Cyclone V SoC in the Cyclone V SoC Power Optimization Application Note available from your local Altera FAE or distributor.