Using the Avery BFM for PCI Express Gen3x16 Simulation on Stratix 10 Devices in Quartus 17.1IR2

Contents

Introduction

Stratix 10 devices support PCI Express Hard IP modes up to Gen3x16. However, the Intel FPGA root complex bus functional model (BFM) only supports modes up to Gen3x8. Simulating Gen3x16 will require the use of a third-party root complex BFM. This document will provide a walkthrough for setting up a simulation using a third-party BFM. The walkthrough will focus on an Avery BFM and is targeted for the Mentor ModelSim and Synopsys VCS simulators. However, the steps could be adapted to other third-party BFMs and other simulation software.

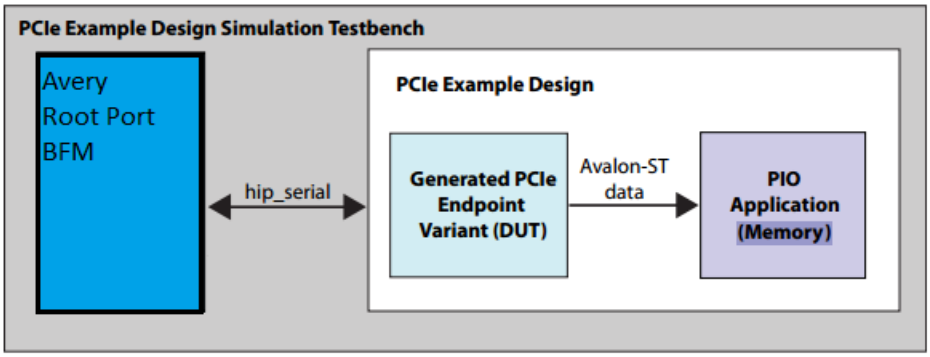
Software Requirements

- Quartus 17.1 IR2 or later
- Mentor ModelSim SE software version 10.3c or later, or Synopsys VCS software version J-2014.12 or later
- Avery BFM 1.8d or later

High Level Overview of Steps

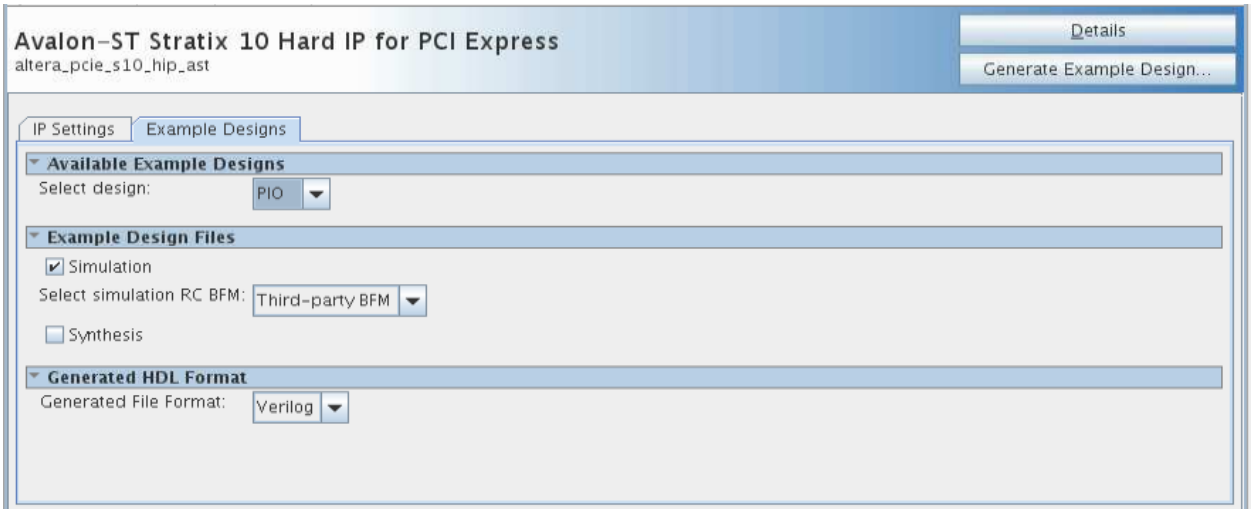
While this walkthrough will be focused on the Avery BFM, using any third-party root complex BFM will require the same basic steps:

1. Create a Gen3x16 design example for simulation
2. Create a file-list of third party BFM files needed for simulation
3. Create a file-list of Gen3x16 design example files needed for simulation
4. Configure the third-party root complex BFM and simulation
5. Modify the Gen3x16 testbench top-level file to incorporate third-party root complex BFM
6. Run the simulation



Step 1: Create the Example Design

1. Copy the static example design archive **ep_g3x16_ast.qar** from the Quartus IP directory to your project folder.
2. Extract the archived project.
3. Open the extracted Qsys system **ep_g3x16_ast.qsys**.
4. Select the **Simulation** option.
5. In the Example Design tab, select **Third-party BFM** from the **Select simulation RC BFM** menu.
6. Click **Generate → Generate HDL,** followed by **Generate → Generate Testbench System**. The folder where you generate the testbench will be referred to as the “example design directory” throughout the rest of this procedure.



Download and Extract the Avery Simulation Scripts

Download the Avery simulation script archive *avery_sim_scripts_171ir2.zip*. Extract the archive to the Example Design Directory. The archive contains:

- pcie_example_design_tb.sv
  - This file is a replacement for the top-level simulation RTL file generated by Quartus. It removes the instantiation of the Intel FPGA root complex BFM, and adds the Avery root complex BFM. Additionally it changes the file format from Verilog to System Verilog, which is important for integrating with the Avery BFM in the VCS simulation.
- apci_top_rc.sv
  - This file is the top-level wrapper for the Avery root complex BFM.
- vcs/
  - *avery_files_vcs.f* – A file-list of all Avery BFM files required by the VCS simulator
  - *ep_g3x16_ast_tb.f* – A file-list of all Quartus Prime Pro Edition software-generated files required by the VCS simulator
  - *vcstest.sh* – A shell script to compile all necessary design files and run the simulation
- modelsim/
  - *avery_files_ms.f* – A file-list of all Avery BFM files required by the ModelSim simulator
  - *msim_setup_avery.tcl* – A TCL simulation script based on the Qsys auto-generated simulation script
  - *mentor.do* – A .do script to configure and run the simulations

Step 2: Create the Avery BFM File List

VCS

The Avery BFM file-list is included with the Avery simulation scripts. The file is called *vcs/avery_files_vcs.f*. Open this file in a text editor and confirm that the file paths match those in your setup. By default, you should not have to make any changes to this file.

ModelSim

The Avery BFM file-list is included with the Avery simulation scripts. The file is called *modelsim/avery_files_ms.f*. Open this file in a text editor and confirm that the file paths match those in your setup. By default, you should not have to make any changes to this file.

Step 3: Create the Example Design File List

VCS

A file list template is included with the Avery simulation scripts (*vcs/pcie_example_design_tb.f*) however many file names are uniquely generated when you create the example design, so you must add the file names yourself.

1. In a text editor, open *vcs/pcie_example_design_tb.f*
2. Also open *pcie_example_design_tb/pcie_example_design_tb/sim/synopsys/vcs/vcs_setup.sh*. This file will contain a list of all design files that need to be compiled for simulation.
3. Scroll through *vcs_setup.sh* until you find the file list. The first file in this list should be *altera_primitives.v* and the last should be *pcie_example_design_tb.v*.
4. Copy this list into the marked area of *vcs/pcie_example_design_tb.f*

```
1
2  -lca
3  -timescale=1ps/1ps
4  -sverilog
5  +verilog2001ext+.v
6  -ntb_opts dtm
7  #INSERT FILE LIST BELOW THIS LINE
8
9  #INSERT FILE LIST ABOVE THIS LINE
10   -top pcie_example_design_tb
11
```

5. Close *vcs_setup.sh*.
6. Replace every instance of $QUARTUS_INSTALL with the absolute or relative path to your Quartus Prime software installation directory. The VCS simulator accepts file lists with absolute or relative paths, but will not accept environment variables.
7. Replace every instance of $QSYS_SIMDIR with the absolute or relative path to your project simulation directory. The VCS simulator accepts file lists with absolute or relative paths, but will not accept environment variables. By default, this address will be *<Example_Design_Directory>/pcie_example_design_tb/ pcie_example_design_tb/sim*.
8. Remove the trailing "\" character from the end of every line in the file list.
9. Remove the final four files from the list (*altpcie_s10_tbed_hwtcl.v*, *altpcied_s10_hwtcl.sv*, *DUT_pcie_tb_ip*, and *pcie_example_design_tb.v*). These files all implement the Intel FPGA root complex BFM and will be replaced by Avery files.
10. In place of these files add *<Example Design Directory>/pcie_example_design_tb.sv*. This is the new top-level file provided with the Avery simulation scripts that will instantiate the Avery BFM.
11. Save and close *pcie_example_design_tb.f*

ModelSim

The ModelSim simulator will compile all required example design files. An example TCL script is included with the Avery simulation scripts (*modelsim/msim_setup_avery.tcl*) however many file names are uniquely generated when you create the example design, so you must modify this TCL script to incorporate the correct file names.

1. Open the *modelsim/msim_setup_avery.tcl* in a text editor.
2. Open the Qsys-generated *msim_setup.tcl* file in a text editor. By default this file will be located at *<Example_Design_Directory>/pcie_example_design_tb/pcie_example_design_tb/sim/mentor*
3. Find the "alias com" sections of both *msim_setup_avery.tcl* and *msim_setup.tcl*. These sections are responsible for compiling all necessary design files.
4. Use copy-paste to replace the "alias com" section of *msim_setup_avery.tcl* with the "alias com" section of *msim_setup.tcl*
5. Close *msim_setup.tcl*
6. Remove the final four files from the "alias com" section of *msim_setup_avery.tcl* (*altpcie_s10_tbed_hwtcl.v*, *altpcied_s10_hwtcl.sv*, *DUT_pcie_tb_ip*, and *pcie_example_design_tb.v*). These files all instantiate the Intel FPGA root complex BFM and will be replaced by Avery files.
7. Save and close *msim_setup_avery.tcl*

Note that unlike with the VCS procedures, you do not need to replace any environment variables or add any new files to the list.

Step 4: Configure the Avery BFM

VCS

In Quartus 17.1IR2, the Avery BFM is configured only to run the simulation in Serial mode. PIPE mode simulation will be available in Quartus 17.1.

To dump the VCS waveform:

1. Open *vcstest.sh* in a text editor.
2. Add the text "+define+APCI_DUMP_VPD -debug_pp" to the vcs command before "+plusarg_save".
3. Save and close *vcstest.sh*.

ModelSim

When using the ModelSim simulator you are required to set some environment variables that are used both to configure the Avery BFM and to run the simulation.

1. Open *modelsim/mentor.do* in a text editor
2. Modify TOP_LEVEL_NAME to match your project. By default, an example design generated by Qsys will have a top level module name of "pcie_example_design_tb.pcie_example_design_tb". Only modify this variable if you have changed the name of the top-level file.
3. Modify QSYS_SIMDIR to match the path to your project's simulation directory. This can be either an absolute path or a relative path. The default value assumes that you unzipped the Avery

simulation files to the Example Design Directory, if you unzipped them elsewhere or made any other changes to the structure/naming of the project then you must change this path.

4. Modify AVERY_PCIE to match the path to the Avery BFM. There is no default value, you must specify this yourself.
5. Modify AVERY_PLI to match the path to the Avery PLI library. There is no default value, you must specify this yourself.
6. Modify USER_DEFINED_ELAB_OPTIONS. By default, these options will reference the PLI library, and instruct elaboration to wait for an available Avery license. Modify this variable only if you need to make changes to these options.
7. To dump the ModelSim waveform, add the text "+define+APCI_DUMP_WLF" to the USER_DEFINED_COMPILE_OPTIONS.
8. Save and close *modelsim/mentor.do*.

Step 5: Modify the Testbench Top-Level File

This has been done for you, and a new top-level file (*pcie_example_design_tb.sv*) is included with the Avery simulation scripts. It has the same name as the old top-level, but instantiates the Avery BFM in place of the Intel FPGA BFM. Additionally, the file format has been changed from Verilog to System Verilog to facilitate integration with the Avery BFM.

For the VCS simulator, you should have added the new top-level to the file list in Step 3. For the ModelSim simulator, the script *mentor.do* will compile the new top-level separately after compiling all other design files.

Step 6: Run the Simulation

VCS

In a terminal with Quartus, VCS, and Avery resources, navigate to *<Example_Design_Directory>/vcs*. Execute the command "/bin/sh vcstest.sh".

ModelSim

In a terminal with Quartus, ModelSim SE, and Avery resources, navigate to *<Example_Design_Directory/modelsim.* Execute the command "vsim -c -do mentor.do".

View Results

This Avery root complex BFM example includes bus enumeration and simple memory transaction test cases. See the *Avery APCIe-Xactor User Guide* for more information on the test cases.

After running the simulation, the simulator should output results indicating whether the test passed, as well as the RX and TX bandwidth.

```
# AVY_INF: apci_test_log@69290.003ns : ----    End testing of test_body (rc) ----
# AVY_INF: apci_test_log@69290.004ns : Test passed
# AVY_INF: apci_test_log@69290.004ns : _____________________________________
# ** Note: $finish    : /tools/apciexactor/1.8d.h1/src/apci_pkg_test.sv(570)
#    Time: 69290004 ps  Iteration: 0  Instance: /pcie_example_design_tb
# AVY_INF: rc@69290.004ns : TX buffers are empty
#
# AVY_INF: rc@69290.004ns : RX: bandwidth 3433.87 mbps, 31 tlps, 688 tlp bytes, 99 dllps, 792 dllp bytes, 1264
0 ts, 384 sos, 0 eieos
# AVY_INF: rc@69290.004ns : TX: bandwidth 4788.86 mbps, 38 tlps, 872 tlp bytes, 149 dllps, 1192 dllp bytes, 12
00 ts, 8 sos, 20 eieos
# End time: 14:45:22 on Apr 17,2017, Elapsed time: 0:18:55
# Errors: 0, Warnings: 1246
```

You can also view the waveforms by opening apci_top.vpd (VCS) or vsim.wlf (ModelSim). The ModelSim waveform below shows the link-training process up to Gen3x16 using the Avery root complex BFM.