This schematic only shows the critical components and traces for a minimum footprint layout. VSENSE, ENABLE, Vout-programming, and other small-signal pins need to be connected and routed according to the customer application.

TP3-TP5 are through-hole test points next to compensation adjust pins. They are used to optimize the control loop if necessary.

For the EN5396Q, Vout and OVP threshold are determined by external R connections to pins 43 and 44 respectively.

Connection determined by customer application.

Css
15n
0402

TP3 TP5 TP4

EN5395Q Voltage Programming Connections

| Voltage Selector | | | Output Voltage |
VS2	VS1	VS0	VOUT
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V
1	1	1	Not Valid

0 = Connect to the GND plane.

1 = Leave open. Pulled high inside the device.

* Not shown. Refer to the datasheet.

U1
EN5395Q/EN5396Q

Pin names (top): NC, NC, NC, M/S, NC, PWM, ENABLE, COMP, EAOUT, EAIN, SS, VSENSE, POK, VS0 / NC, VS1 / XOV, VS2 / XFB

Left pins 1–13: NC

Right pins: 42 NC, 41 NC, 40 AGND, 39 AVIN, 38 ROCP, 37 NC, 36 NC, 35 PVIN, 34 PVIN, 33 PVIN, 32 PVIN, 31 PVIN, 30 PVIN

Bottom pins 14–20: VOUT; 21 NC, 22 NC, 23 NC, 24 PGND, 25 PGND, 26 PGND, 27 PGND, 28 PGND, 29 PGND, 59 PGND
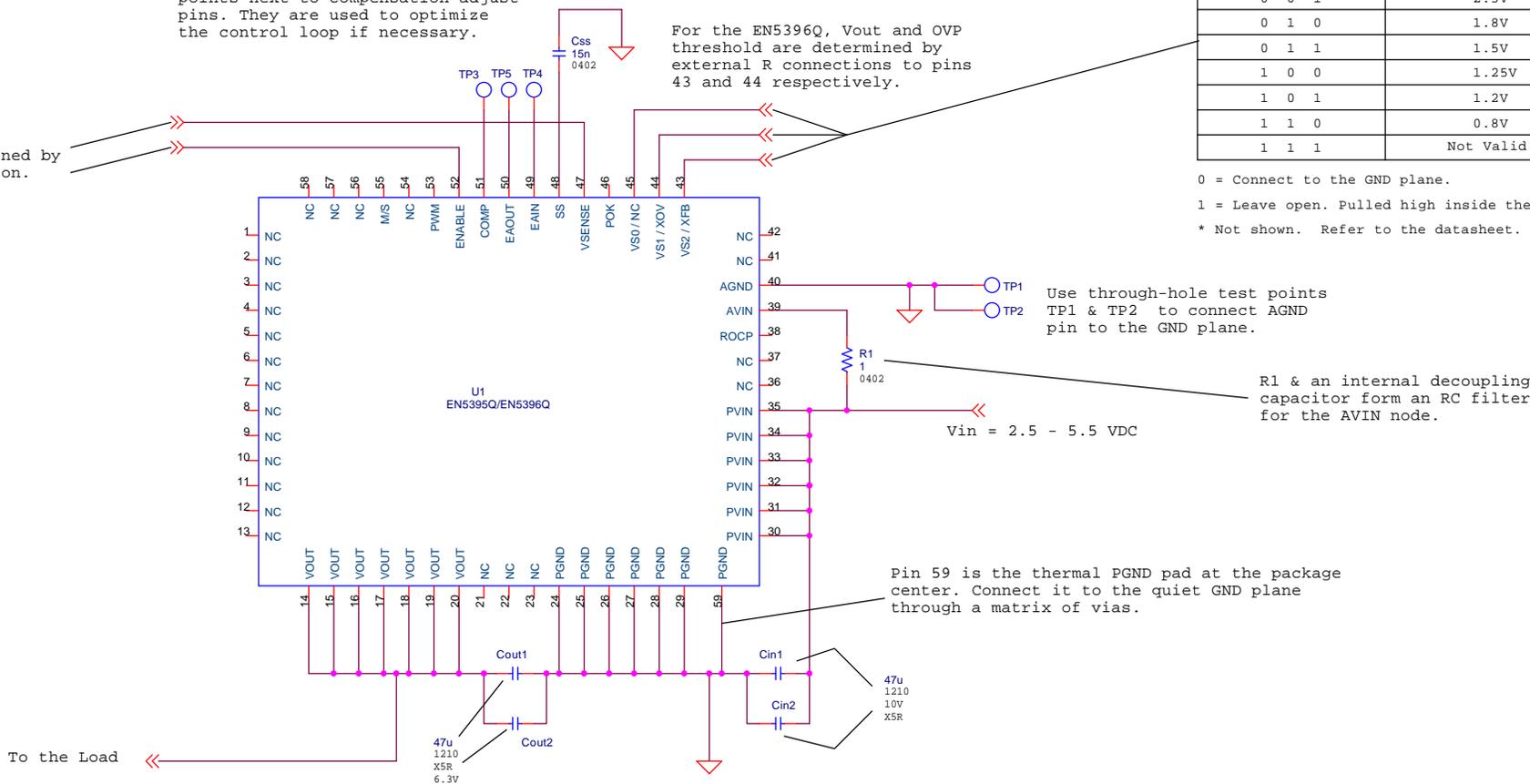
TP1
TP2
Use through-hole test points TP1 & TP2 to connect AGND pin to the GND plane.

R1
1
0402

R1 & an internal decoupling capacitor form an RC filter for the AVIN node.

Vin = 2.5 - 5.5 VDC

Pin 59 is the thermal PGND pad at the package center. Connect it to the quiet GND plane through a matrix of vias.

Cout1

Cin1

47u
1210
10V
X5R

Cin2

47u
1210
X5R
6.3V

Cout2

To the Load

This connection to the GND plane is the via matrix in the thermal pad in addition to the two rows of vias by Cin & Cout.
(Please see the Gerber files.)