Intel Releases New PCI Express* Connector Metrology Collateral in Support of PCI Express 3.0

Intel is committed to clear, accurate, and accessible connector metrology that meets the needs of the PCI Express 3.0 interconnect. Intel has upgraded its PCIe* connector measurement reference design and procedures to extend accuracy of measurement to the higher frequencies required of PCIe 3.0 connectors.

Intel is releasing three items to support the new PCIe 3.0 connector performance requirements:

PCI Express 3.0 Connector High Speed Connector Evaluation Board (CEB) Reference Design*

PCI Express 3.0 Connector High Speed Electrical Test Procedure*

PCI Express 3.0 Generic Support Bracket Design for Connector Evaluation Board*

This reference design and the associated test procedure update and replace the previously released PCIe connector evaluation board to accurately measure PCIe connector performance to 3.0 limits.

The current Connector Evaluation Board (CEB) designs are for measuring performance of PCIe 1.0 and PCIe 2.0 connectors. The PCIe 1.0 and PCIe 2.0 board designs contain many permutations of via/pad/anti-pad and add-in card pad sizes. The PCIe 1.0 and PCIe 2.0 board calibration structures are designed to provide accurate measurements to 3 X Nyquist, 3.75 GHz and 7.5 GHz for PCIe 1.0 and PCIe 2.0 boards, respectively.

The new PCIe 3.0 board is designed to evaluate PCIe connectors to PCIe 3.0 limits. The PCIe 3.0 board contains a single x4 PCIe footprint with standard via/pad/anti-pad and add-in card pad sizes. The calibration structures on the PCIe 3.0 board are designed to provide accurate measurements to 3 x PCIe 3.0 Nyquist frequencies (12 GHz). A comparison of the new features to the previous release is shown in Table 1.

Table 1: Comparison of PCIe Connector Metrology Characteristics and Features

Existing PCIe Connector Metrology	New PCIe Connector Metrology
PCIe 1.0 and PCIe 2.0 connector evaluation board, multiple-sites/multiple add-in cards	PCIe 3.0 connector evaluation board, single-site/single add-in card
Polyclad* 370 PCB	Nelco* N4000-SI*/Nelco N4000-13 SI
Measure to 4 GHz	Measure to 40 GHz
SOLT, TRL Calibration	TRL calibration
3.0 CEB, 3.0 CEB BOM, 3.0 Support Bracket	CEB, CEB bill of materials, support bracket
	Characterization board design rules

PCIe 3.0 Measurement Collateral

The complete PCIe 3.0 collateral consists of the measurement procedure and the CEB design files. The measurement procedure (*PCI Express* 3.0 Connector High Speed Electrical Test Procedure*) includes the CEB bill of materials and a measurement template. The board design file (*PCI Express* 3.0 Connector High Speed Connector Evaluation Board (CEB) Reference Design*) includes a Cadence* board design file, fab drawing, and stack-up information needed to fabricate and assemble the connector evaluation board. There is also a generic bracket design to support the CEB while testing, *PCI Express* 3.0 Generic Support Bracket Design for Connector Evaluation Board*. This bracket can be used with all Intel PCIe 3.0 connector evaluation boards. All of this collateral con be found on Intel.com: (http://www.intel.com/technology/pciexpress/devnet/resources.htm)

Connector Verification

Connector performance verification is an important step to reliable, high speed interconnects. Although it is expected that many PCIe connectors will meet 3.0 performance expectations, measuring the connector performance, or reviewing connector measurements provided by the supplier or a third party is the best means of understanding the characteristics of any one specific PCIe connector. In the long term, Intel encourages suppliers and customers to standardize a path for ensuring connector compliance to PCIe 3.0 performance requirements. Intel hopes that the PCIe 3.0 connector measurement procedure and evaluation board will help Intel, suppliers, and customers to begin the discussion. Intel will require its PCIe 3.0 connector vendors to comply with the measurement procedure, *PCI Express* 3.0 Connector High Speed Electrical Test Procedure.*