PCI Express* 3.0 Connector High Speed Electrical

Test Procedure

Revision 002

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Revision History

Revision	Revision History	Date
001	• Initial release of the document.	January 2011
002	• Corrected PCI Express name.	February 2018

1 Introduction

This test procedure outlines the steps required to perform high speed integrity measurements on a PCI Express* connector at 8 GT/s. The high speed signal integrity requirements are described in the connector specification section (Chapter 5) of the *PCI Express* Card Electromechanical (CEM) Specification*. Intel also has an 8 GT/s PCI Express connector evaluation board set available for use for performing this test procedure [*PCI Express* 3.0 Connector High Speed Connector Evaluation Board (CEB) Reference Design*]. The procedures in this test document use the CEB design.

1.1 Reference Documents

This document follows the procedures outlined in these documents:

- *EIA 364-101 – Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems*
- *EIA 364-90 - Cross Ratio Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection systems*
- *EIA 364-108 – Impedance, Reflection Coefficient, Return Loss and VSWR Measured in the Time and Frequency domain Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems*
- *EIA 364-23B – Low Level Contact Resistance Test Procedures for Electrical Connectors and Sockets*
- *EIA 364-70B – Termperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets*
- *IEEE* P802.3ap/Draft 3.3 – Draft Amendment of IEEE Standard for Information Technology*
- Agilent* application note, “Stripline TRL Calibration Fixtures for 10-Gigabit Interconnect Analysis”, ©Agilent Technologies, Inc, 5989-4897EN, April 5, 2006
- K. Vaz, M. Caggiano “Measurement Technique for the Extraction of Differential S-Parameters from Single-Ended S-Parameters,” IEEE 27th Spring Seminar on Electronics Technology, 2004
- D. Bockelman, W. Eisenstadt “Combined Differential and Common-Mode Scattering Parameters: Theory and Simulation,” IEEE Transactions on Microwave Theory and Techniques, VOL 43, NO. 7, July 1995.

- *PCI Express Card Electromechanical Specification*, Revision 2

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2 Equipment List

The following list of equipment is adequate for measurement accuracy. The equipment has been verified to be compatible with this test procedure and the test fixture.

Vector Network Analyzer:	Agilent N5230A or Anritsu* MS4640A Series or Rhode and Schwartz* ZVB 20 or equivalent
Coaxial Terminators:	50 Ω, VSWR ≤ 1.2 at 20 GHz
50 Ω Coaxial cables:	Gore* CAB062707-0250Ω or Rosenberger* or equivalent

The coaxial terminations have a direct effect on the results of the measurements. The performance of the coaxial termination across the measurement frequency range must be verified before proceeding.

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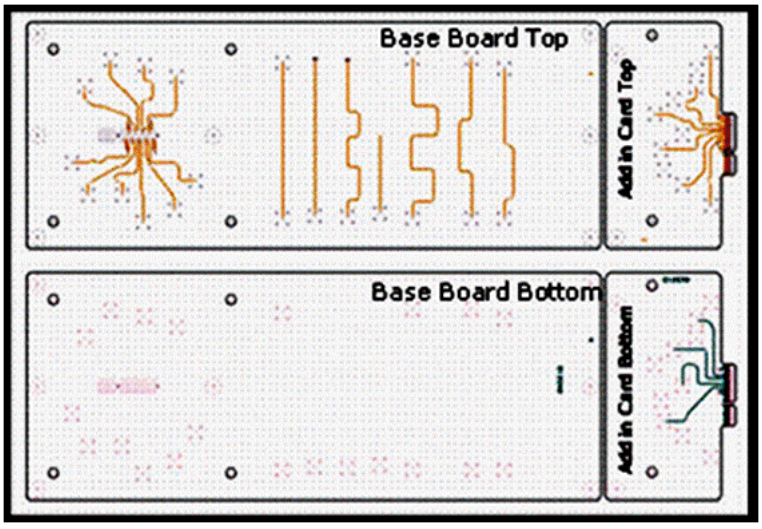
3 Test Board Set Description

This test procedure is developed for use with the 8 GT/s PCI Express Connector Evaluation Board Set [*PCI Express* 3.0 Connector High Speed Connector Evaluation Board (CEB) Reference Design*] shown in Figure 3-1. The test fixture is designed and should be built to specific criteria, as described below, to ensure good measurement accuracy and compatibility with the interconnect specification. The connector evaluation board set includes:

- Microstrip signal launch on baseboard
- PCIe* connector on baseboard
- Through-Reflect-Load (TRL) calibration kit
- Microstrip signal launch on add-in card

Figure 3-1. PCIe Connector Evaluation Board Set

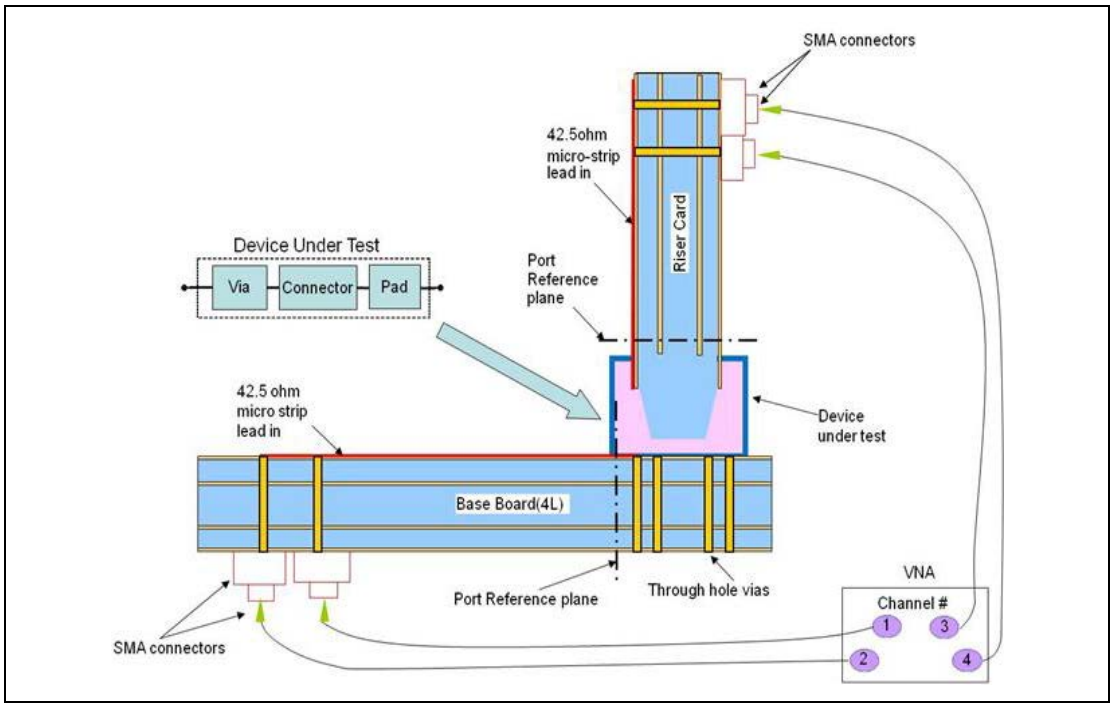


A TRL calibration kit is included on the connector evaluation board. Reference designs including baseboard stack-up, DUT description, and riser card stack-up information are provided upon request to Intel through the Resource and Design Center (RDC).

Figure 3-2 describes the details of the 4-layer baseboard, Device Under Test (DUT) and riser card test set up. A 3 board array typically fits a 21” x 24” panel at ≥7 degree fiber rotation. Board finish should

be immersion silver with exception of the edge fingers on the add-in card. The edge fingers should be plated with 20 – 50 microinches gold over a minimum 150 microinches nickel.

Figure 3-2. VNA Setup with Device Under Test



Make sure signal traces are not plated with nickel or gold. The setup for evaluating the connector electrical performance includes the following characteristics detailed in Appendix B: General Connector Evaluation Board Design Guidelines.

The vector network analyzer setup used in this procedure performs S-parameter measurements using an 85 ohm differential reference impedance. Therefore, all of the test traces must be held to a characteristic impedance of 42.5 ohms +/- 5%. The test board is a four layer stack-up of Nelco* 13 core material and Nelco 13-SI* prepreg. The stack-up details are shown in Figure 3-3.

Figure 3-3. PCIe Connector Evaluation Board Set Stack-Up (Identical Stack-Up for Baseboard and Add-In Card)

Layer Name	Plane Description	Layer Thickness (mil)	Copper Weight (oz)	Dielectric Er (@ 10 GHz)	Single Ended Impedance Tolerance	Differential Impedance Tolerance
	solder mask	0.5				
1	SIGNAL	1.9	0.5 *		<+/- 5%	<+/- 5%
	Nelco 13 SI	3		3.3		
2	GND	1.3	1			
	Nelco 13	49 (ADJUST CORE THICKNESS TO ACHIEVE OVERALL BOARD THICKNESS SPECIFICATION)		3.6		
3	GND	1.3	1			
	Nelco 13 SI	3		3.3		
4	SIGNAL	1.9	0.5 *		<+/- 5%	<+/- 5%
	solder mask	0.5				
	Overall Board Thickness with solder mask	62.4	* 3 oz before plating			

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4 Vector Network analyzer Settings

The state of the vector network analyzer (VNA) affects the measurement and calibration performance. In order to improve accuracy and repeatability for connector measurements, it is necessary to use these baseline settings in combination with the calibration procedure.

Table 4-1. VNA Settings for Measuring PCIe Connectors

VNA Setting	Value
Frequency Range	≤ 50 MHz to 20 GHz
Number of Points	≥ 2000
Number of averages	3
IF Bandwidth	1 kHz

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5 Calibration

5.1 Reference Plane

To properly characterize the performance of the connector in the test fixture, the VNA must be calibrated to a known standard. The intent of the calibration is to eliminate systematic errors in the measurement and improve measurement accuracy.

The precise geometric location at which a vector network analyzer measurement is made is called the reference plane. There are sometimes two different reference planes involved in a connector measurement. If a commercial coaxial calibration kit is used, it will typically establish a reference plane near the end of the test cables. In this case, a second step, called de-embedding, is needed to remove the influence of the test fixture and move the reference plane closer to the DUT. Some calibration methods can place the reference plane near the connector without this second step.

One key property of the reference plane is that it is to be far enough from features such as vias, that ephemeral modes die out before reaching the reference plane. The mounting vias are to be measured as part of the DUT. It is recommended that the reference plane be positioned in signal lines at about 50mils from the connector vias and 50 mils from the edge finger pads

5.2 Four Port Calibration

TRL is the recommended method for calibration (see Appendix C: TRL Calibration Kit, for specific calibration constants). TRL has the advantage that it can be easily tailored to impedances other than 50 ohms and can eliminate the need for de-embedding the test fixture. It has the disadvantage that it is not available on all machines, and it is not familiar to as many users as other calibration methods.

5.3 Verification of Calibration

Calibration should be tested to verify quality. The calibration should be reliable to at least 12 GHz. Calibration reliability is tested by measuring the primary through of the calibration structures. Ideally, the Primary through measurement should produce 0 dB at all frequencies in the measurement range. In practice, calibration will produce deviation from zero, reliable calibration will produce less than 1% deviation from 0 dB [approximately 0 ± 0.086 dB] at all frequencies below 8 GHz, and

within 2% of 0 dB [approximately 0 ± 0.170 dB] between 8 and 12 GHz. Measurements should be reported through 20 GHz.

5.4 System Reference Impedance

Warning: Some tools do not correctly handle S parameters with reference impedances other than 50 ohms. If you are using a reference impedance other than 50 ohms, check that the tool correctly recognizes the reference impedance used in the measurement.

Helpful tips:

- Make a copy of the Touchstone file.
- Edit the R parameter to change the stated reference impedance.
- Reload the data into the tool.
- Check that the tool recognizes the change by comparing insertion loss plots.
- If the tool recognizes the change, the tool is working correctly. If the tool does not recognize the change, the data must be normalized to 50 ohm reference impedance before using the tool.
- The reference impedance is the impedance of the TRL calibration lines on the board, which may not be 50 ohms. The VNA may report a default value of 50 ohms regardless of the TRL line impedance. If the VNA does not report the correct reference impedance, edit the touchstone file so that it accurately states the correct reference impedance.
- Always distribute data files normalized to 50 ohm reference impedance.

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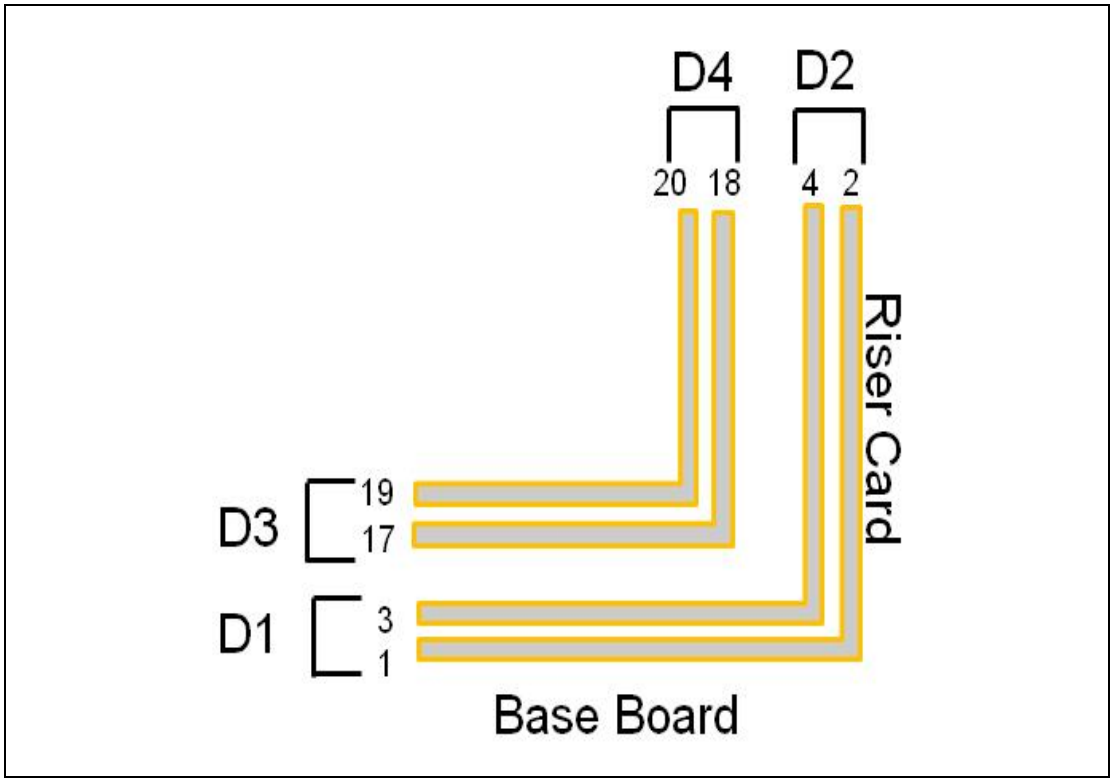
6 Insertion and Return Loss Measurements

6.1 Port Naming Convention

Insertion and return loss are multi-port measurements using the port naming convention in Figure 6-1.

Figure 6-1. Single Ended and Differential (DD) Port Naming Convention as Defined by the PCIe CEM Specification



All nearby differential pairs other than those being measured need to be terminated. Since precision wide band 42.5 ohm resistors do not exist, adjacent ports can be terminated with 50 ohm terminators.

6.2 Differential Insertion Loss (DDS21)

Differential inserion loss is calculated using Equation 1 shown where S is formatted as a complex number.

Equation 1. Calculation of Differential Insertion Loss DDS21 (Figure 6-1, D1 to D2)

$$DDS21(f) = 20\log_{10} [|(S21 - S23 - S41 + S43)/2|]$$

6.3 Differential Return Loss (DDS11)

Differential return loss is calculated using Equation 2 shown below where S is formatted as a complex number.

Equation 2. Calculation of Differential Insertion Loss DDS11 (Reference Figure 6-1, D1)

$$DDS11(f) = 20\log_{10} [|(S11 - S13 - S31 + S33)/2|]$$

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7 Crosstalk Measurement

7.1 Victim-Aggressor-Ground Pattern

Near-end crosstalk, NEXT, is crosstalk where both the driven aggressor and the victim are on the base board side, or both are on the add-in card. Differential-differential crosstalk is crosstalk where the aggressor is driven differentially and the signal at the victim is read differentially.

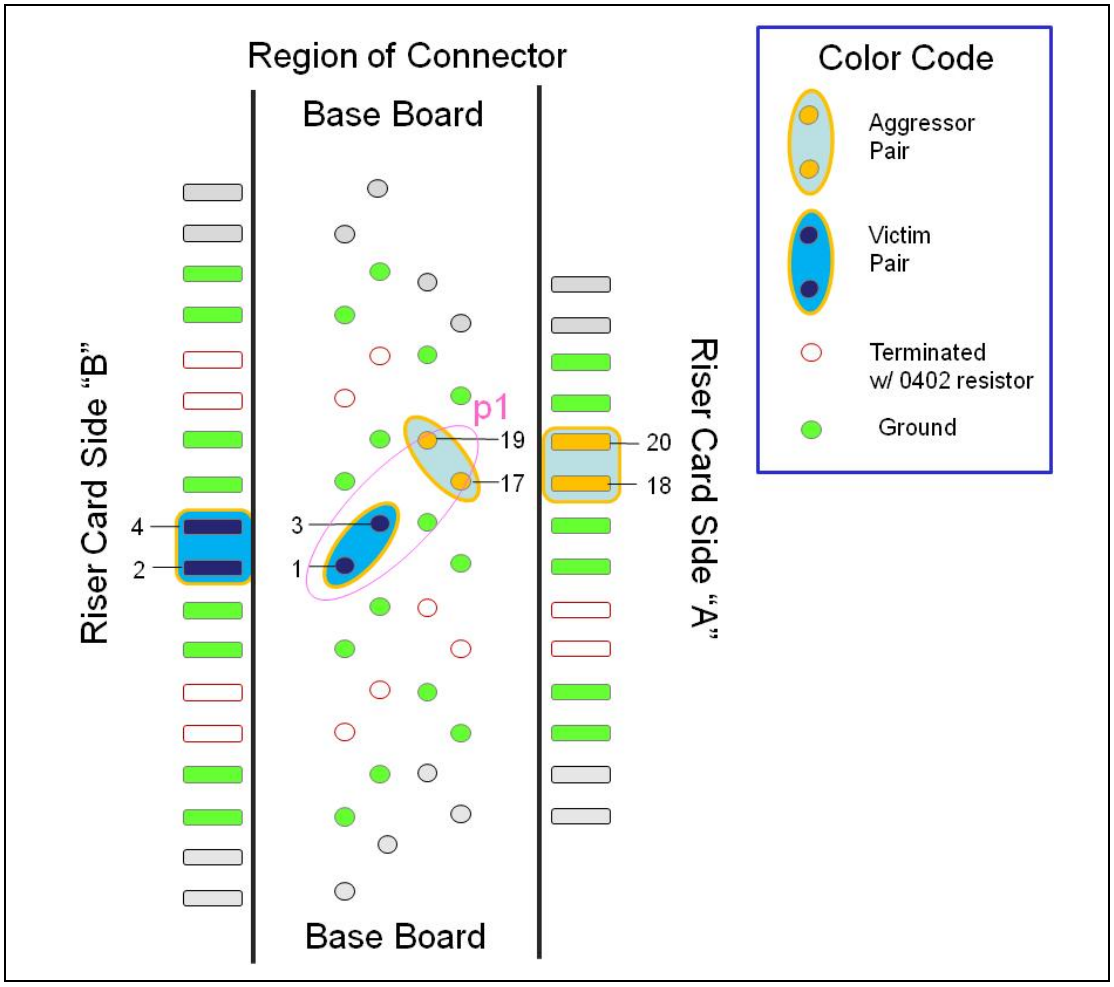
Far-end crosstalk, FEXT, is crosstalk where the driven signals and the measured signals are on opposite ends of the connector. It is to be measured using the same conditions described above for near-end crosstalk.

In evaluating crosstalk, it is acceptable to take advantage of symmetries that might be found in the connector, such as the left and right sides being identical.

For each pair that is to be characterized, called the signal pair, there will be several adjacent pairs that contribute crosstalk. These contributors will be called aggressors.

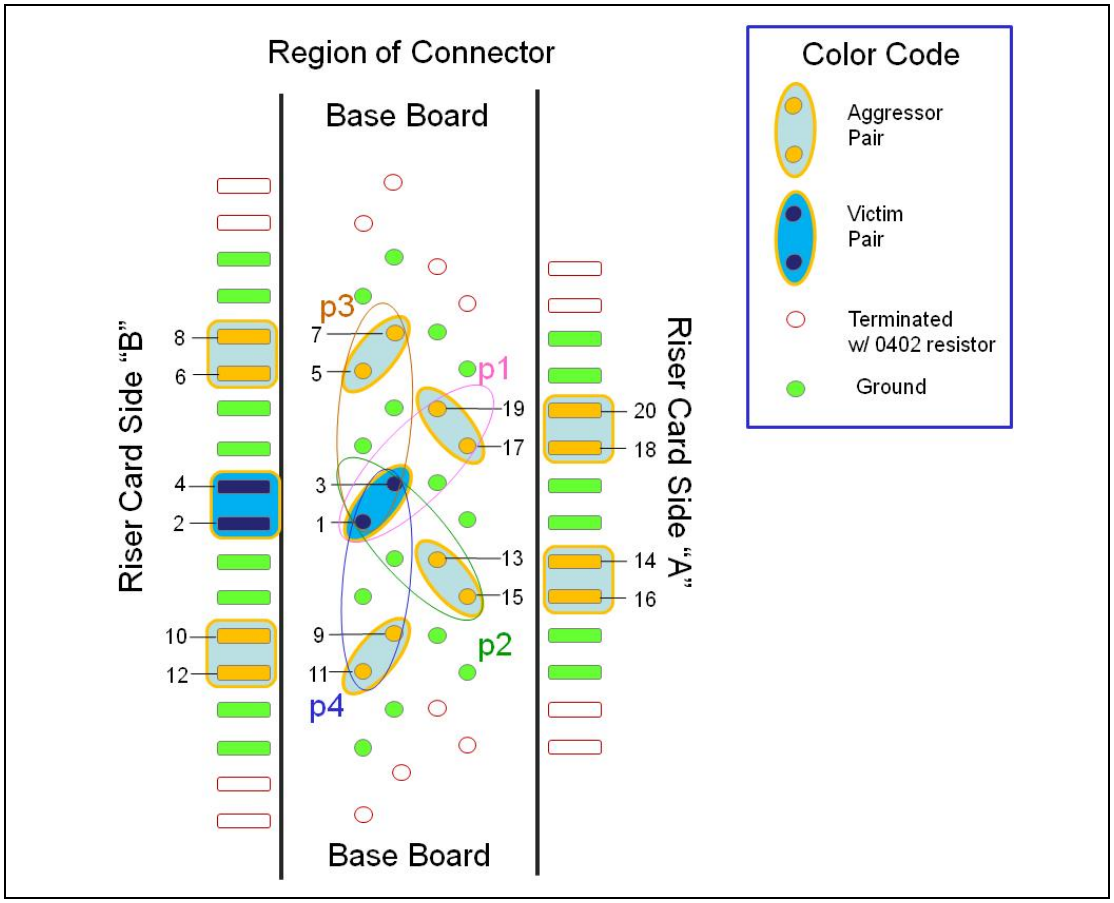
The PCIe standard method of summing connector crosstalk is a differential vector sum of all adjacent pairs as near end aggressors. The differential multi-active method differs from the standard method by summing connector crosstalk as a power sum using opposite side adjacent pairs as near end aggressors and same side adjacent pairs as far end aggressors. The differential multi-active method accounts for the directionality of aggressors and removes sensitivity to phase, see Figure E-1. Differential Multi-Active Crosstalk (DDXTK_ma) Summation Example.

Figure 7-1. Port Definition Diagram for Differential Single Aggressor Near End Crosstalk (DDNEXT_sa)



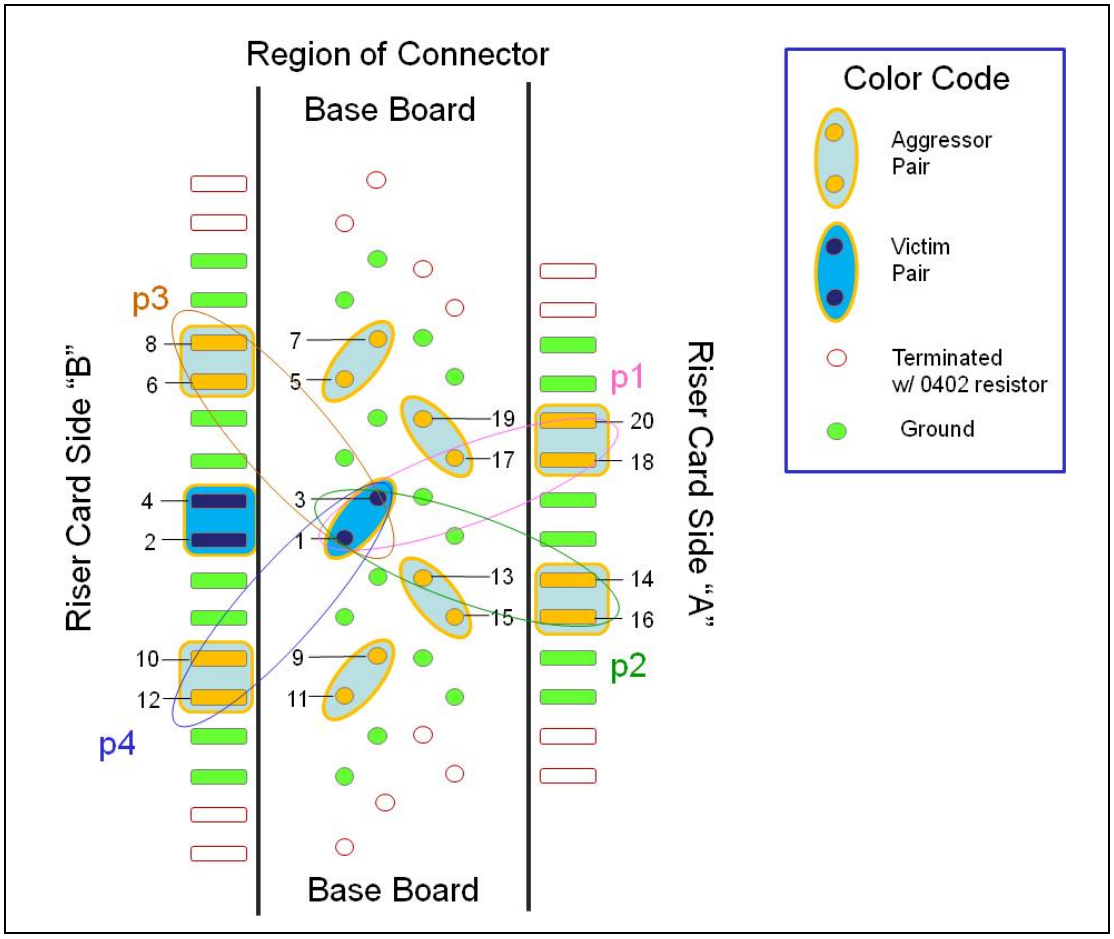
Termination can be achieved with SMA terminators or 0402 resistors.

Figure 7-2. Port Definition Diagram for Differential Multiple Aggressor Near End Crosstalk (DDNEXT)



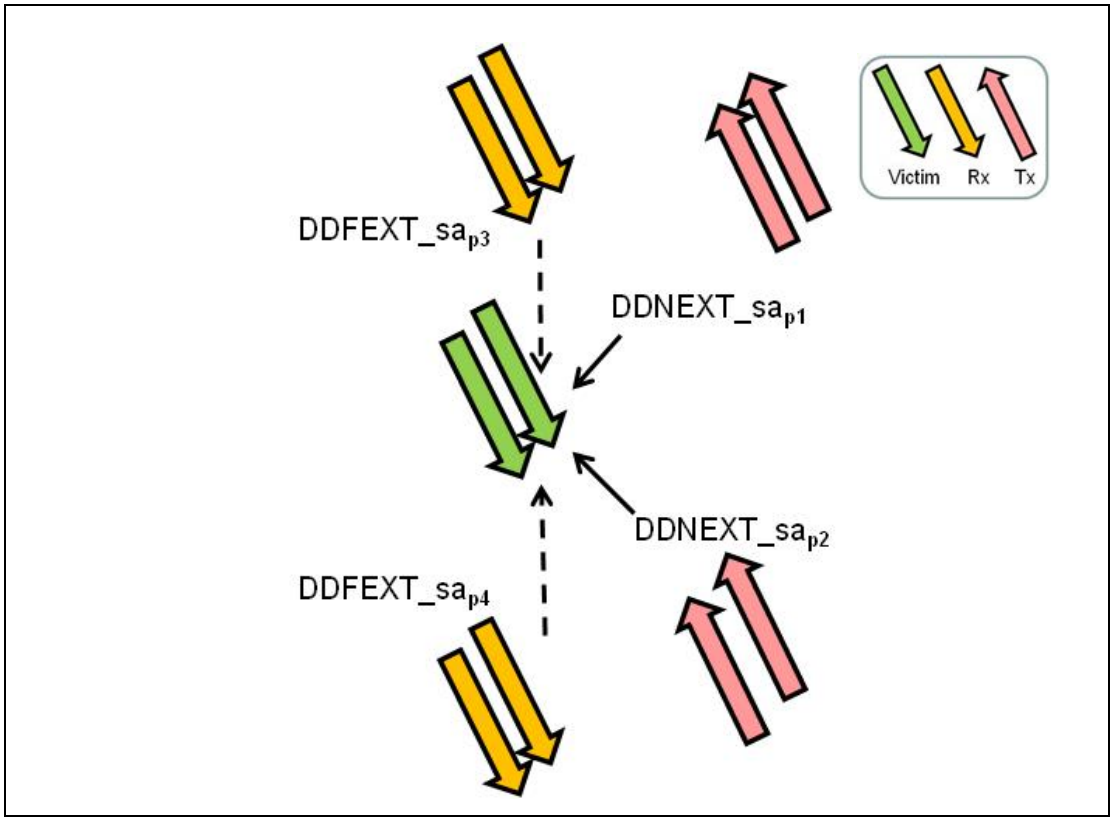
Termination can be achieved with SMA terminators or 0402 resistors depending on whether the positions will be used for differential multiple aggressor crosstalk measurements or not.

Figure 7-3. Port Definition Diagram for Differential, Multiple Aggressor, Far End Crosstalk (DDFEXT)



Termination can be achieved with SMA terminators or 0402 resistors depending on whether the positions will be used for multiple aggressor crosstalk measurements or not.

Figure 7-4. Crosstalk Components for Differential Multi-Active Crosstalk (DDXTK_ma) Signals



7.2 Differential Near End Crosstalk

7.2.1 Single Aggressor DDNEXT

Differential single aggressor near end cross talk (DDNEXT_sa) on the victim differential pair is calculated using port assignments defined in Figure 6-1 and Equation 3 through Equation 6 shown where S is formatted as a complex number.

Equation 3. Calculations of Differential Single Aggressor Near End Crosstalk DDNEXT_sa from Single Ended Measurements (Reference Figure 7-2)

$$DDNEXT_sa_{p1}(f) = (S_{1_17} - S_{3_17} - S_{1_19} + S_{3_19})/2$$

Equation 4. Calculations of Differential Single Aggressor Near End Crosstalk DDNEXT_sa from Single Ended Measurements (Reference Figure 7-2)

$$DDNEXT_sa_{p2}(f) = (S_{1_15} - S_{3_15} - S_{1_13} + S_{3_13})/2$$

Equation 5. Calculations of Differential Single Aggressor Near End Crosstalk DDNEXT_sa from Single Ended Measurements (Reference Figure 7-2)

$$DDNEXT_sa_{p3}(f) = (S_{1_5} - S_{3_5} - S_{1_7} + S_{3_7})/2$$

Equation 6. Calculations of Differential Single Aggressor Near End Crosstalk DDNEXT_sa from Single Ended Measurements (Reference Figure 7-2)

$$DDNEXT_sa_{p4}(f) = (S_{1_11} - S_{3_11} - S_{1_9} + S_{3_9})/2$$

7.2.2 Multiple Aggressor DDNEXT

Multiple aggressor differential near end cross talk (DDNEXT) on the victim differential pair is calculated as a vector sum using Equation 7 shown where DDNEXT(f) is expressed in dB.

Equation 7. Vector Sum of Differential Multiple Aggressor Near End Crosstalk from Single Aggressor S-Parameter Measurements (Reference Figure 7-2)

$$DDNEXT(f) = 20\log_{10}\left(\left| \sum_{n} DDNEXT_sa_{pn} \right| \right) \Big|_{n=1,2,3,4}$$

7.3 Differential Far End Crosstalk#

The # is for reporting purposes only.

7.3.1 Single Aggressor DDFEXT

Differential single aggressor far end cross talk (DDFEXT_sa) on the victim differential pair is calculated using port assignments defined in Figure 6-1 and Equation 8 through Equation 11 shown where S is formatted as a complex number.

Equation 8. Calculations of Differential Single Aggressor Far End Crosstalk DDFEXT_sa from Single Ended Measurements (Reference Figure 7-3)

$$DDFEXT_sa_{p1}(f) = (S_{1_18}-S_{3_18}-S_{1_20}+S_{3_20})/2$$

Equation 9. Calculations of Differential Single Aggressor Far End Crosstalk DDFEXT_sa from Single Ended Measurements (Reference Figure 7-3)

$$DDFEXT_sa_{p2}(f) = (S_{1_16}-S_{3_16}-S_{1_14}+S_{3_14})/2$$

Equation 10. Calculations of Differential Single Aggressor Far End Crosstalk DDFEXT_sa from Single Ended Measurements (Reference Figure 7-3)

$$DDFEXT_sa_{p3}(f) = (S_{1_6}-S_{3_6}-S_{1_8}+S_{3_8})/2$$

Equation 11. Calculations of Differential Single Aggressor Far End Crosstalk DDFEXT_sa from Single Ended Measurements (Reference Figure 7-3)

$$DDFEXT_sa_{p4}(f) = (S_{1_12}-S_{3_12}-S_{1_10}+S_{3_10})/2$$

7.3.2 Multiple Aggressor DDFEXT

Differential multiple aggressor far end cross talk (DDFEXT) on the victim differential pair is calculated as a vector sum using Equation 12 shown. DDFEXT(f) is expressed in dB.

$$DDFEXT(f) = 20\log_{10}\left(\left|\sum_{m} DDFEXT_sa_{pm}\right|\right)\Big|_{m=1,2,3,4}$$

Equation 12. Vector Sum of Differential Multiple Aggressor Far End Crosstalk from Single Aggressor S-Parameter Measurements (Reference Figure 7-4)

7.4 Multi-Active Crosstalk (DDXTK_ma)#

The # is for reporting purposes only.

7.4.1 Multiple Aggressor DDNEXTγ

Total differential multiple aggressor near end cross talk on the victim differential pair is calculated as a power sum using Equation 13 shown below. DDNEXTγ is expressed in dB.

Equation 13. Power sum of differential multiple aggressor near end crosstalk DDNEXTγ from single aggressor S-parameter measurements (Reference Figure 7-4)

$$DDNEXT_{\gamma}(f) = 10\log_{10}\left(\sum_{n}|(DDNEXT(f)_sa_{pn})|^{2}\right)\Big|_{n=1,2}$$

7.4.2 Multiple Aggressor DDFEXTγ

Total differential multiple aggressor far end cross talk on the victim differential pair is calculated as a power sum using Equation 14 shown below. DDFEXTγ is expressed in dB.

Equation 14. Power Sum of Differential Multiple Aggressor Far End Crosstalk DDFEXTγ from Single Aggressor S-Parameter Measurements (Reference Figure 7-4)

$$DDFEXT_{\gamma}(f) = 10\log_{10}\left(\sum_{m}|(DDFEXT(f)_sa_{pm})|^{2}\right)\Big|_{m=3,4}$$

7.4.3 Multi-Active Crosstalk (DDXTK_ma)

Differential, multi-active, cross talk on the victim differential pair is calculated as a power sum using Equation 14 shown below. DDXTK_ma is expressed in dB.

Equation 15. Power Sum of Differential Multi-Active Crosstalk DDXTK_ma from Single Aggressor S-Parameter Measurements (Reference Figure 7-4)

$$DDXTK_ma(f) = 10\log_{10}\left(\sum_{n}10^{DDNEXT\gamma(f)/10} + \sum_{m}10^{DDFEXT\gamma(f)/10}\right)\Big|_{m=3,4}^{n=1,2}$$

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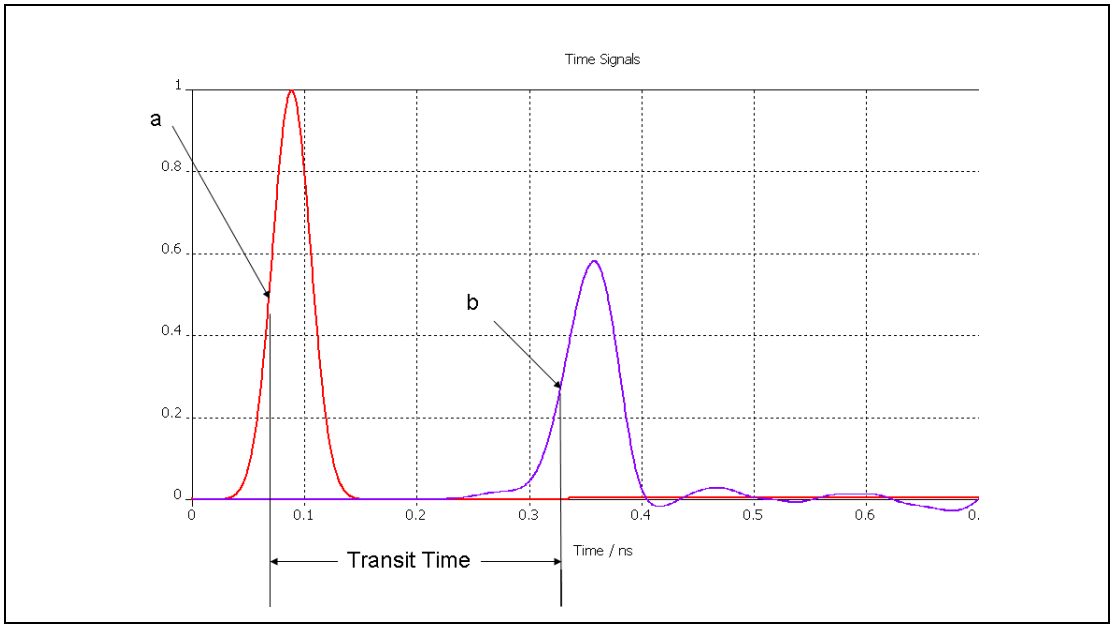
8 Skew Measurement

8.1 Skew Definition

Published skew may be established from simulations wherein the insertion and return loss simulations show correlation to measurement.

Figure 8-1. Illustration of How Transit Time is Measured on a Single Trace



Multiple transit time measurements are used to establish skew. Transit time is defined as time b – time a, where the input pulse is at 50% of the driving voltage at the leading edge of the pulse and the output pulse is at 50% of the exiting voltage at the leading edge of the pulse.

8.2 Skew Measurement

The measurement of an individual trace is at 50% of the driving voltage (point a) and at 50% of the exiting voltage (point b). Transit time through the connector is the difference between b and a. Skew is the difference in transit time between the two traces of a pair.

Measured skew is preferred to simulations when available.

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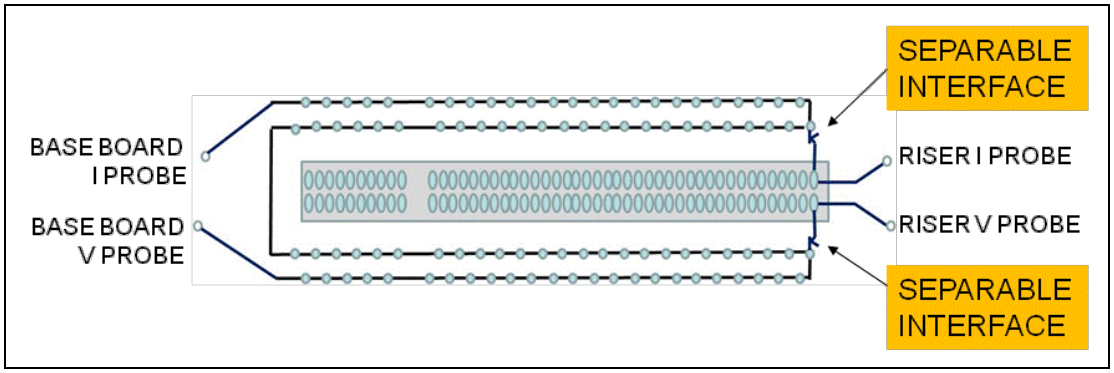
9 Low Level Contact Resistance

Low Level Contact Resistance (LLCR) measurements should be made using the four wire method detailed in EIA 364-23B. Use the daisy chain design illustrated in Figure 9-1.

Figure 9-1. Daisy Chain Pattern for Connector LLCR Measurement



The contact resistance measurement should include the solder tail, baseboard via and the contact mating interface.

Test voltage: 20 mV maximum open circuit

Test current: 100 mA maximum

Number of readings: 500 minimum

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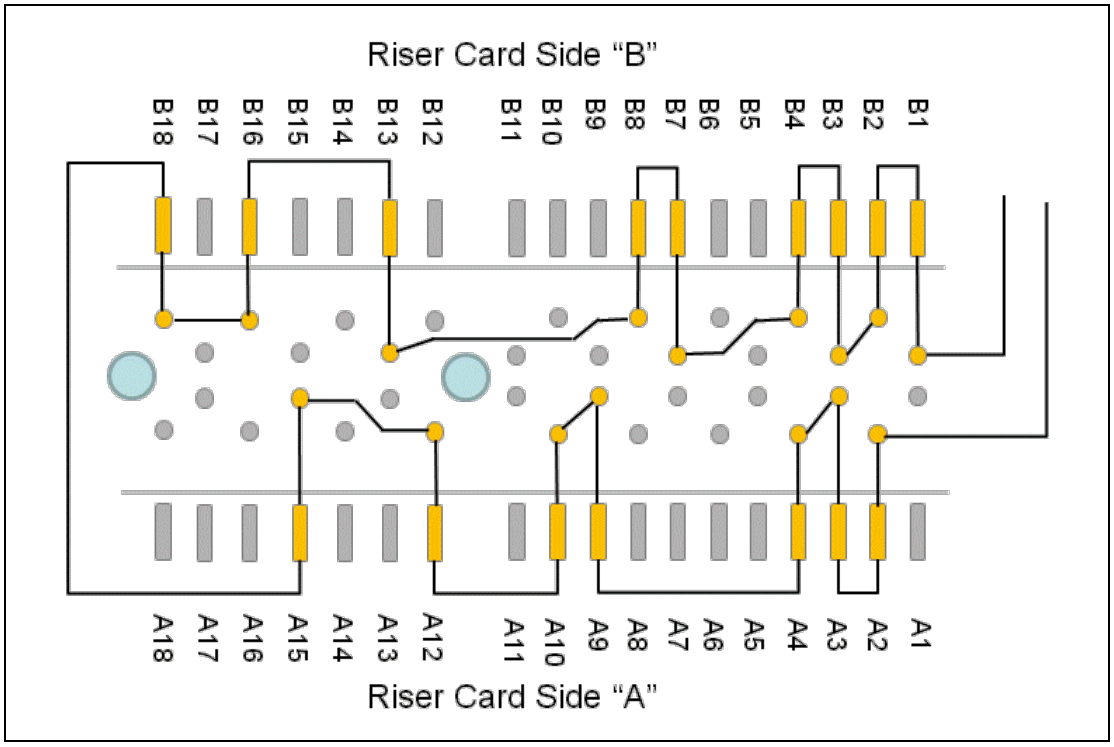
10 Contact Current Rating

Contact current rating should be made using the four wire method detailed in EIA 364-23B. Use the daisy chain design illustrated in Figure 10-1.

Figure 10-1. Daisy Chain Pattern for Contact Current Rating



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A Connector Evaluation Board Bill-of-Materials

Table A-1. Bill of Materials for PCIe 3.0 Connector Evaluation Baseboard and Add-In Card

Component	Part number, Description	Quantity
Baord to Board Connector	PCIE Express connector, 64 position	1
Calibration Resistor	0201 resistor, 85 Ω ± 2 Ω	4
TerminationResistor	0402 resistor, 42.5 Ω + 7 Ω - 0 Ω	8
RF Connector	Rosenberger 32K153-400LS	31
PC Board	Connector Evaluation Base Board, 4 layer, Nelco N4000-13/Nelco N4000-13 SI	1
PC Board	Connector Evaluation Add-In Card, 4 layer, Nelco N4000-13/Nelco N4000-13-SI	1

NOTE: PC boards are available as part of the *PCI Express* 3.0 Connector High Speed Connector Evaluation Board (CEB) Reference Design*.

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B General Connector Evaluation Board Design Guidelines

1. TRL Calibration Structure Guidelines
   a. The total thickness of the test fixture PCB is 1.57 mm (0.625”) +-0.006”.
   b. The test add-in card is a break-out card fabricated in the same PCB panel for the fixture. This ensures the dielectric material properties of add-in card and test fixture card are same.
   c. The measurement signals are launched into the connector from the top of the test fixture, including the through-hole stub effect.
   d. Traces between the DUT and measurement ports (SMA or microprobe) should be uncoupled from each other, as much as possible.
   e. The trace lengths between the DUT and measurement ports are identical and as short as possible.
   f. The trace lengths between the DUT and measurement port on the test baseboard and add-in card should be routed to a length “L1”, within ±0.0005” of one another.

Note: The edge finger pad is not counted as the add-in card PCB trace; it is considered as a part of the connector interface.

   g. All of the traces on the test board and add-in card must be held to a characteristic impedance of 42.5 ohms +/-5% (2.125 ohms)
   h. The test add-in card edge finger is 165 mils long and 28 mils wide. The ground plane immediately underneath the edge finger pads is removed to minimize the capacitive effect of the edge finger.
   i. Use the PCI-SIG* recommended size of the anti-pad corresponding to the plated through holes on the test board is 58 mils in diameter. Use the PCI-SIG recommended size of pads on the plated through holes of 42 mils in diameter and the plated through holes themselves are 28 mils finished. There is no thermal relief on the plated through holes connection to the ground/power planes. Remove pads on inner layers.

j. SMA land – use the land pattern footprint optimized for high speed performance.

k. Avoid silkscreen over trace.

l. Avoid placing any structure, line, or element over the trace outside the break-out region.

m. Route the trace on the microstrip.

n. Maintain ≥ 0.750″ SMA center-to-center distance on each board and on assemblies of two boards.

o. Use Nelco 13/Nelco 13-SI and fiber weave mitigation design by rotating artwork ≥ 7″.

p. Place TRL calibration structures on the same board as the connector under test.

2. TRL Calibration Structure Guidelines

Note: "Through" structures are for TRL calibration.

a. Primary Through Trace: length = (length of trace from the connector under test to the SMA, minus the distance to reference plane, typically 50 mils) times 2, i.e., (2*L1) – 0.100"

b. Secondary Through #1 Trace: length = Primary Through length + 1989 mils (covers 300 MHz – 1.240 GHz using Nelco13/Nelco13-SI stack-up)

c. Secondary Through #2 Trace: length = Primary Through length + 480 mils (covers 1.240 GHz – 5.150 GHz using Nelco13/Nelco13-SI stack-up)

d. Secondary Through #3 Trace: length = Primary Through length + 116 mils (covers 5.150 GHz – 20 GHz using Nelco13/Nelco13-SI stack-up)

e. Short Trace: short to the GND plane, length is half the length of the primary through

f. Load Trace #1: long line (within reason – For example, 3.5" – 5"), and at the end of the line, put two 85 ohm resistors in parallel to ground using very small resistors (e.g., 0201)

g. Load Trace #2: long line (within reason – For example, 3.5" – 5"), and at the end of the line, put two 85 ohm resistors in parallel to ground using very small resistors (e.g., 0201)

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C TRL Calibration Kit

A TRL calibration kit designed to remove the test fixture effect from the S-parameter measurement are included in the connector evaluation board design using the standards shown below.

Crossover Frequencies

DC – 0.300 GHz	Load #1 and Load #2
0.300 – 1.240 GHz	Secondary Through #1
1.240 GHz – 5.150 GHz	Secondary Through #2
5.150 GHz – 20 GHz	Secondary Through #3

Applicable to connector evaluation board stack-up defined in Figure 3-3.

Typical Offset Time (time will vary depending on value of Er)

86 ps	Secondary Through #1
21 ps	Secondary Through #2
5 ps	Secondary Through #3

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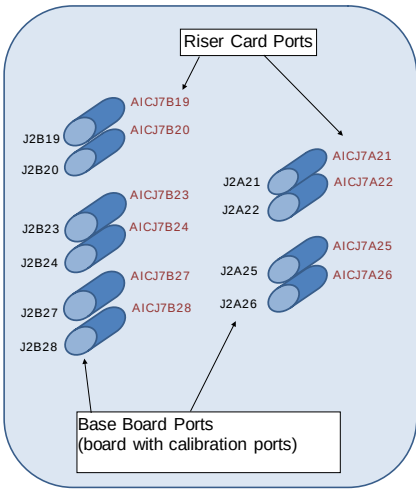
D Typical VNA Measurement Template

Figure D-1. Data Collection Template for 4-Port VNA Measurements

Equip	Test #	Base Board Site #	Port1	Port2	Port3	Port4	Test Type
VNA	1	J2	J2B23	J2B24	J2B19	J2B20	NEXT
VNA	2	J2	J2B23	J2B24	AICJ7B19	AICJ7B20	FEXT
VNA	3	J2	J2B23	J2B24	J2B27	J2B28	NEXT
VNA	4	J2	J2B23	J2B24	AICJ7B27	AICJ7B28	FEXT
VNA	5	J2	J2B23	J2B24	J2A21	J2A22	NEXT
VNA	6	J2	J2B23	J2B24	AICJ7A21	AICJ7A22	FEXT
VNA	7	J2	J2B23	J2B24	J2A25	J2A26	NEXT
VNA	8	J2	J2B23	J2B24	AICJ7A25	AICJ7A26	FEXT
VNA	9	J2	J2B23	J2B24	AICJ7B23	AICJ7B24	IL / RL
VNA	10	J2	J2A25	J2A26	J2A21	J2A22	NEXT
VNA	11	J2	J2A25	J2A26	AICJ7A21	AICJ7A22	FEXT
VNA	12	J2	J2A25	J2A26	AICJ7A25	AICJ7A26	IL / RL
VNA	13	J2	J2B27	J2B28	AICJ7B27	AICJ7B28	IL / RL
VNA	14	J2	J2B19	J2B20	AICJ7B19	AICJ7B20	IL / RL



The 4-port VNA measurement template applicable to port designations as defined on the Intel PCIe Add-in Card [available as part of the *PCI Express* 3.0 Connector High Speed Connector Evaluation Board (CEB) Reference Design*].

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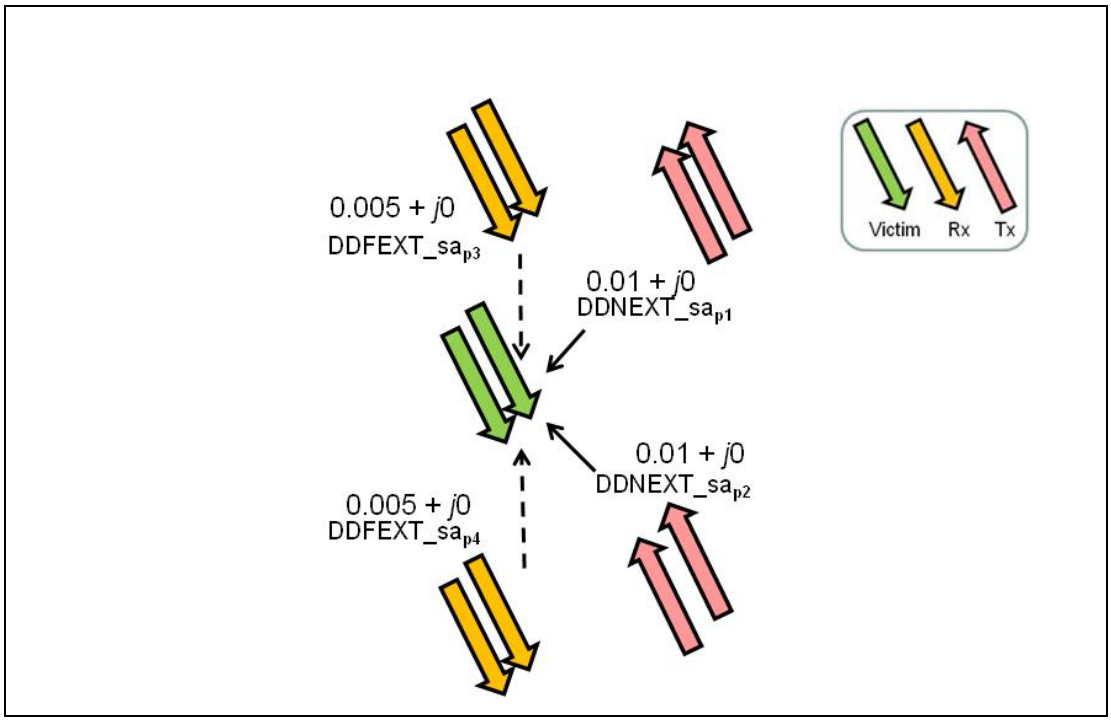
E DDXTK_ma Example

Figure E-1. Differential Multi-Active Crosstalk (DDXTK_ma) Summation Example



In the example above, at a frequency f, same-side, differential DDFEXT single-aggressors of (0.005+*j*0) and opposite-side, differential DDNEXT single-aggressors of (0.01+*j*0), result in DDXTK_ma of -33 dB as shown in the calculation below:

$DDNEXT\gamma(f)_{1,2} = 10\log_{10}(\Sigma(|(0.01+j0)|^2+|(0.01+j0)|^2)) = 10\log_{10}(0.0002) = -37$ dB

$DDFEXT\gamma(f)_{3,4} = 10\log_{10}(\Sigma(|(0.005+j0)|^2+|(0.005+j0)|^2)) = 10\log_{10}(0.00005) = -43$ dB

$DDXTK_ma(f) = 10\log_{10}(10^{(-37/10)} + 10^{(-43/10)})$

$DDXTK_ma(f) = 10\log_{10}(0.0002 + 0.00005)$

$DDXTK_ma(f) = 10\log_{10}(0.00025)$

$DDXTK_ma(f) = -36$ dB

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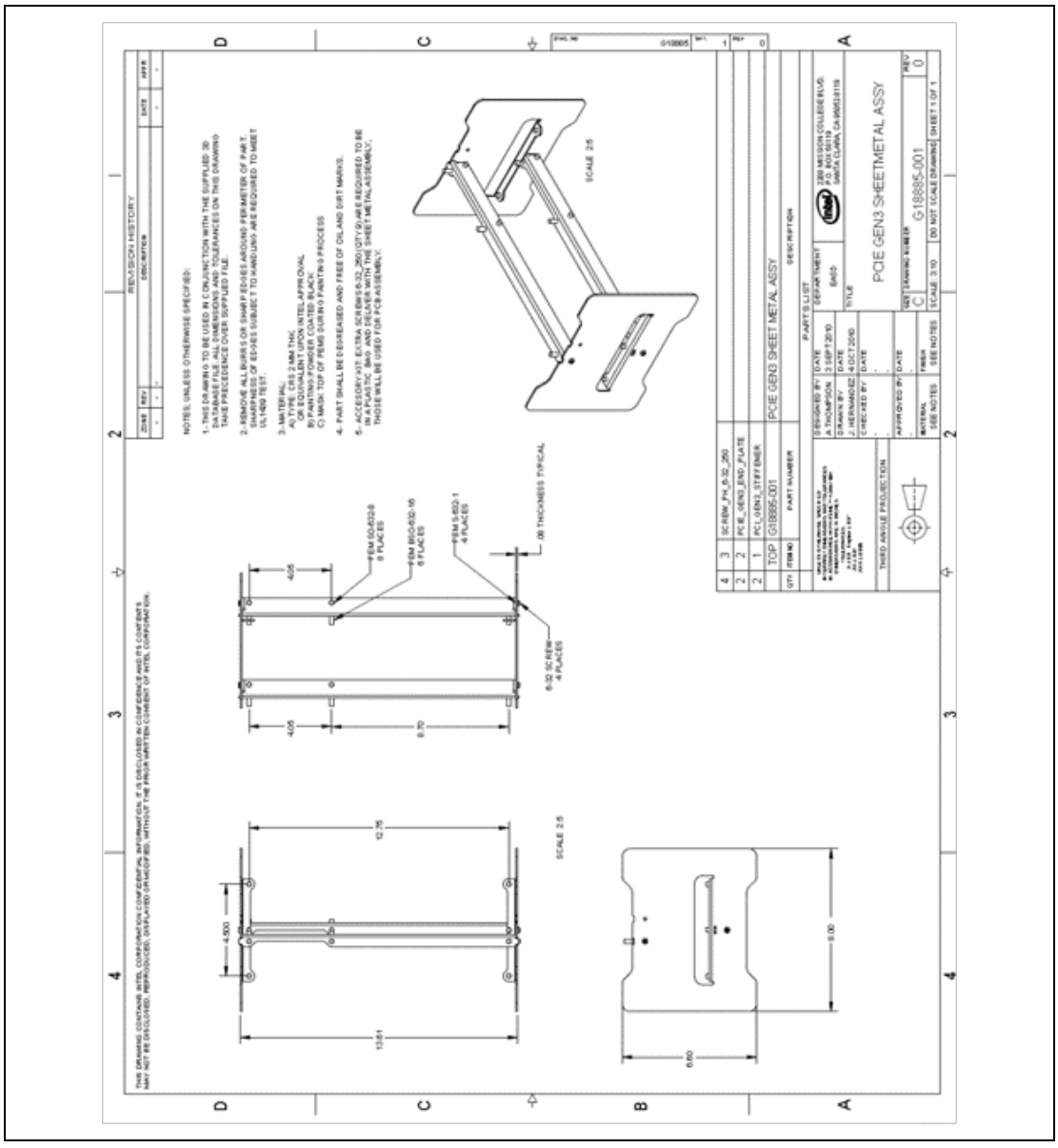
F Add-In Card and Baseboard Support Bracket Drawing

Figure F-1. Support Bracket Drawing for PCIe Connector Evaluation



NOTE: Available as Intel Generic Support Bracket Design for Connector Evaluation Boards.

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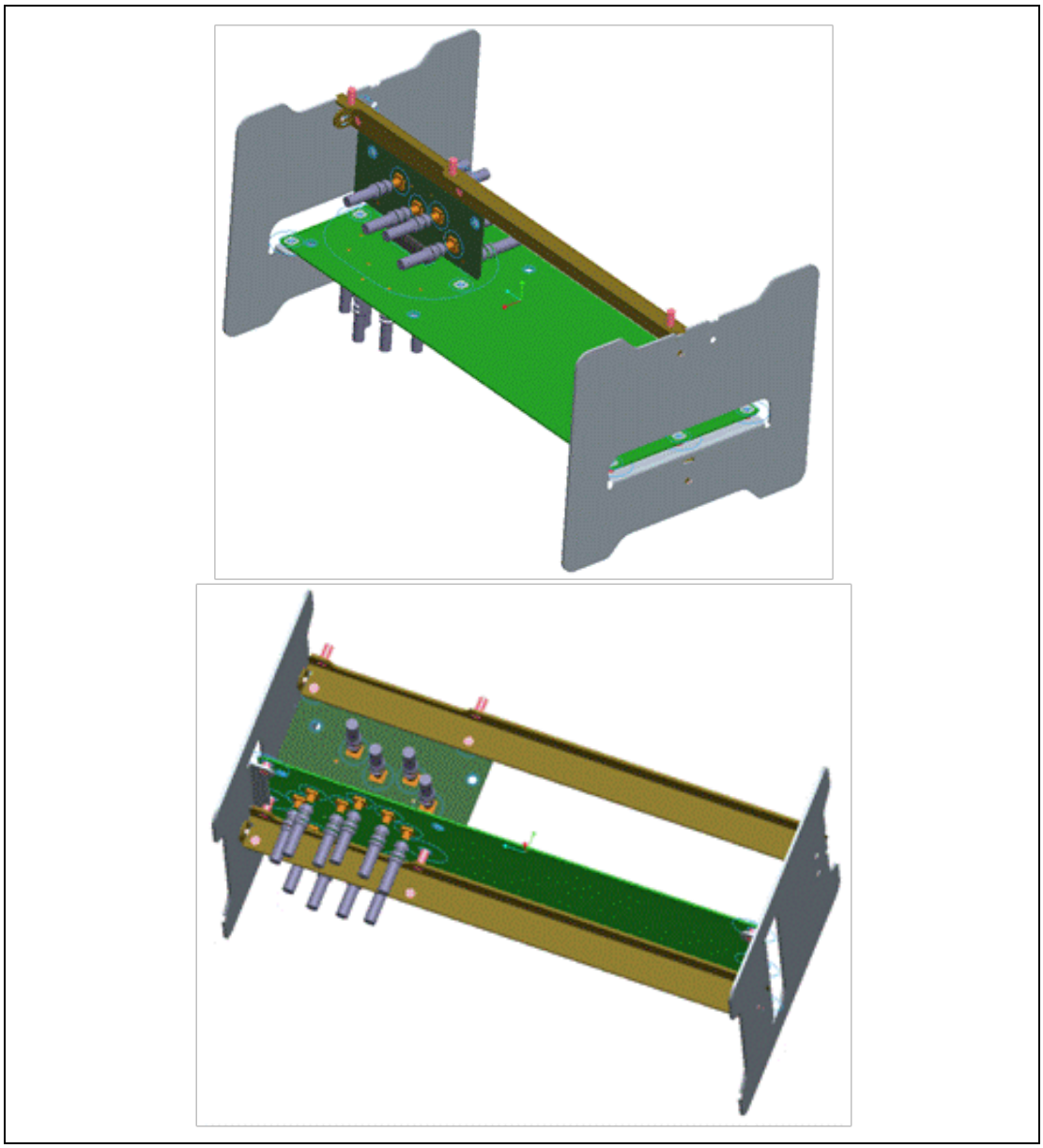
G Add-In Card and Baseboard Assembly

Figure G-1. PCIe Connector Evaluation Board and Support Bracket



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